Practitioner's Docket No. HK9225US (formerly 25857) ***PATENT***

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Yang et al. Confirmation No.: 4487

Application No.: 10/725,933 Group No.: 2891

Filed: December 3, 2003 Examiner: David A. Zarneke

For: FAN OUT TYPE WAFER LEVEL PACKAGE STRUCTURE AND METHOD OF THE SAME

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF PRIOR INVENTION IN THE UNITED STATES OR IN A NAFTA OR WTO MEMBER COUNTRY TO OVERCOME CITED PATENT OR PUBLICATION (37 C.F.R. § 1.131)

PURPOSE OF DECLARATION

1. This declaration is to establish completion of the invention of this application in the United States at a date prior to January 22, 2002, that is the effective date of the prior art publication that was cited by the examiner.

2. The persons making this declaration are the inventors.

CERTIFICATION UNDER 37 C.F.R. §§ 1.8(a) and 1.10*

*(When using Express Mail, the Express Mail label number is **mandatory**; Express Mail certification is optional.)*

I hereby certify that, on the date shown below, this correspondence is being:

MAILING

__ deposited with the United States Postal Service in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

37 C.F.R. § 1.8(a)
__ with sufficient postage as first class mail.

37 C.F.R. § 1.10*
__ as "Express Mail Post Office to Addressee"
Mailing Label No. _____ **(mandatory)**

TRANSMISSION

__ facsimile transmitted to the Patent and Trademark Office, (571) 273 - 8300.

Laura K Cahill
Signature

Date: November 9, 2006

Laura K. Cahill
(type or print name of person certifying)

** Only the date of filing (' 1.6) will be the date used in a patent term adjustment calculation, although the date on any certificate of mailing or transmission under ' 1.8 continues to be taken into account in determining timeliness. See ' 1.703(f). Consider "Express Mail Post Office to Addressee" (' 1.10) or facsimile transmission (' 1.6(d)) for the reply to be accorded the earliest possible filing date for patent term adjustment calculations.*

FACTS AND DOCUMENTARY EVIDENCE

3. To establish the date of completion of the invention of this application, the following attached documents and/or models are submitted as evidence:

sketches
blueprints
photographs
reproduction(s)of notebook entries
model
supporting statement(s) by witness(es) (where verbal disclosures are the evidence relied upon)
interference testimony
disclosure documents

From these documents and/or models, it can be seen that the invention in this application was made at least by the date of Sep. 6, 2001, which is a date earlier than the effective date of the reference.

DILIGENCE

4. Attached is a statement establishing the diligence of the applicants, from the time of their conception, to a time just prior to the date of the reference, up to the filing of this application.

TIME OF PRESENTATION OF THE DECLARATION

5. This declaration is submitted with the first response after final rejection, and is for the purpose of overcoming a new ground of rejection or requirement made in the final rejection.

DECLARATION

6. As a person signing below:

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURE(S)

Wen-Kun Yang

Inventor's signature: _____

Date: Sept. 11, 2006 Country of Citizenship: Taiwan, R.O.C.

Residence: _____

Post Office Address: No.65, Kuang-Fu North Rd., Hsin-chu Industrial Park
Hu-kou, Hsin-chu 303, Taiwan, R.O.C.

Wen-Pin Yang

Inventor's signature: W. P. Yang

Date: Sept 11, 2006 Country of Citizenship: Taiwan, R.O.C.

Residence: _____

Post Office Address: No.65, Kuang-Fu North Rd., Hsin-chu Industrial Park
Hu-kou, Hsin-chu 303, Taiwan, R.O.C.

Shih-Li Chen

Inventor's signature: Shih-li Chen

Date: Sep. 11, 2006 Country of Citizenship: Taiwan, R.O.C.

Residence: _____

Post Office Address: No.65, Kuang-Fu North Rd., Hsin-chu Industrial Park
Hu-kou, Hsin-chu 303, Taiwan, R.O.C.

Affidavit of Facts

We, Wei-Ming Lee, Shih-Li Chen, W. P. Yang are inventors of the pending case 10/725, 933 of ACE (Advanced Chip Engineering Inc.), a company organized under laws of Taiwan, R.O.C., and having a business address of No 65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu 303, Taiwan.

We hereby attest that the solder layer 12 in the Taiwan patent '766 is used due to the first material layer is too thick and the first opening is too small, and the electroplating can not make sure the reliability test. Thus, the solder 12 is used in the initial development. However, we found that the solder 12 will cause the bubble issue on Sept. 2003, please refer to the SEM photo of figure 1 of the attachment one. Therefore, solder layer 12 is removed and first contact conductive layer is used (refer to figure 2) in order to solve the "bubble issue" that may causing the reliability problem.

Therefore, we replace the solder layer 12 in the above patent during the development on Dec. 2003, the reason to remove solder layer "12" includes (refer to figure 2):

- The thickness of layer "122" can be thinner. (Ex. SINR material)
- The diameter of hole of "116" is too small, and can not get the good quality during stencil printing of solder paste.
- '766 can not avoid the "Bubble" inside the hole after printing the solder which will cause the reliability problem during temperature cycling test.
- Reduce process step to save cost.
- E-Plating has better contact quality.

We hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issue thereon.

Signature Wei-Ming Lee, Shih-Li Chen, W. P. Yang

Date 10/20/06

Attachment One:

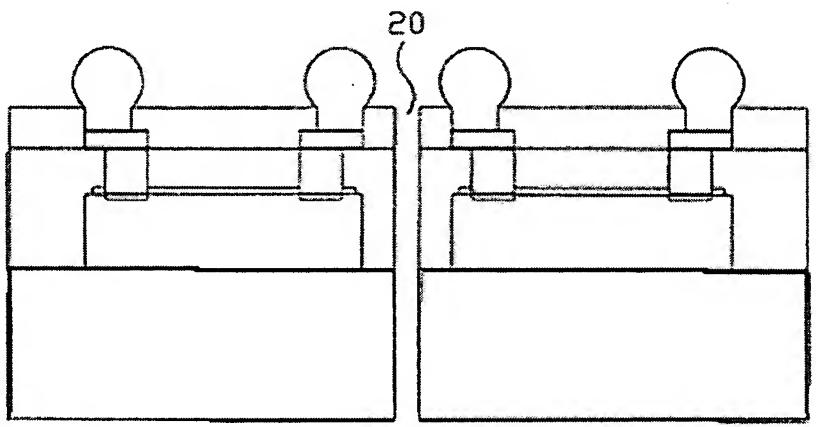
Comments by W.K. Yang on
Taiwan Patent No. 177,766 and
U.S. Patent Application No. 10/725,933

Fan-out WLP Attachment one

Advanced Chip Engineering Technology

Analysis by WK Yang

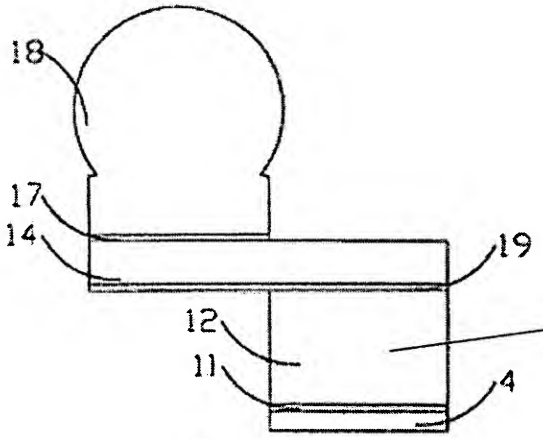
Taiwan 766 Patent



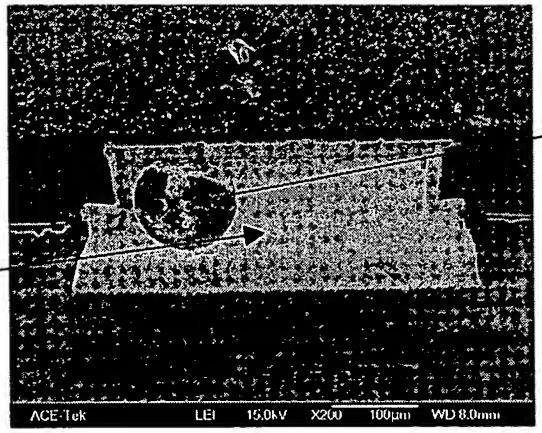
圖十三

Figure 1

The "bubble" is generated in the solder layer and it is getting worse when the opening is narrower.

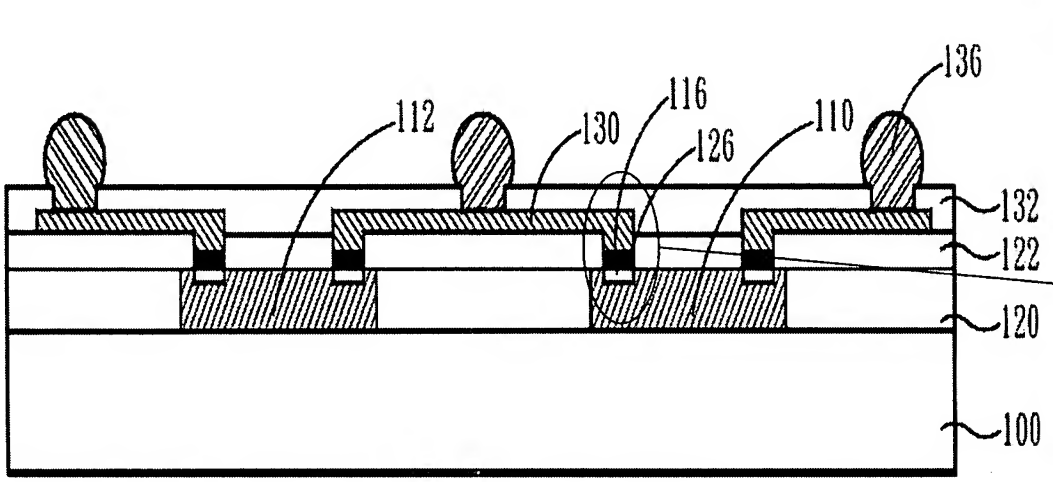


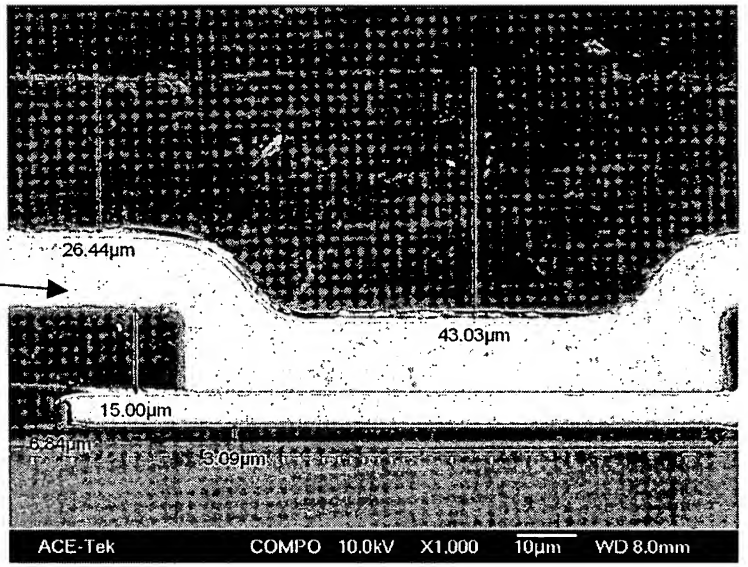
圖十四



bubble

P1305-30US (U.S. Patent Application No. 10/725,933)



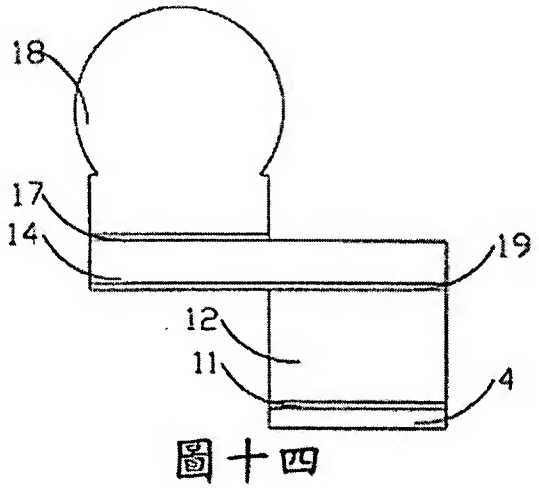


The reason to remove solder layer "12":
-The thickness of layer "122" can be thinner. (Ex. SINR material)
-The diameter of hole of "116" is too small, and can not obtain good quality
-It needs stencil printing for solder paste.
-Can not avoid the "Bubble" inside the hole after printing the solder which will cause the reliability problem during thermal procedure.
-Reduce process step to save cost.
-E-Plating has better solution.

Figure 2

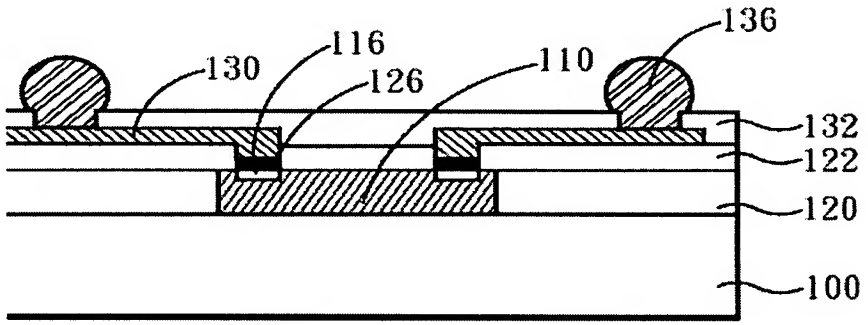
Comparison

Taiwan Patent No. 177,766



圖十四

U.S. Patent Application No. 10/725,933



The major difference of inter-connecting are
-766 patent has the metal layer **"12"** that is Solder paste by stencil printing
-766 patent has the seed metal **"19"** Ti/Cu over the opening

EXHIBIT A

Doc No	File (File Date)	Date	Testimony of Custodian or Qualified Witness
1	Weekly report ww11_2001.doc 2006.6.23	Mar. 16th, 2001	The Reporter: Willy Liaw
	Weekly report ww14_2001.doc 2006.6.23	Apr. 2nd, 2001	The Reporter: Willy Liaw
2	FO-WLP patent document to patent lawyer	Sep. 6th, 2001	
3	WAFER LEVEL PACKAGING (FAN.PPT) 2001.9.6	Sep. 6th, 2001	File Author: Wen-kun Yang
	FO-WLP patent document to patent lawyer WLP-FAN OUT.XLS 2001.9.2	Sep. 2nd, 2001	File Author: Wen-kun Yang File Receiver: Vincent Chiang
3-1	Official Document of Taiwan IPO (includes the Application and Certificate)	Sep. 25th, 2001	
4	New_Technology.ppt 2002.1.15	Jan. 15th, 2002	File Author: Wen-kun Yang
5	WEEKLY REPORT FOR 40TH WEEK.DOC 2002.10.8	Oct. 8th, 2002	Reporter: Roger Chiu
	ROGER_REPORT_1.DOC 2002.12.16	Dec. 16th, 2002	Reporter: Roger Chiu
6-1	714_2003.doc	Jul. 14th, 2003	Conferee: Wen-kun Yang, DC Huang, Co Co Kow, Kathy Lin, Ben Lin, Chairman: Bob Chen Conference Recorder: Bob Chen Copy Receiver: David Lin, Jalex Sun, MJ Chiu
6-2	Weekly Report 030.doc	Jul. 21st ~Jul. 25th,	File Author: Bob Chen
6-3	PROJECT CODE_2003.DOC 2003.7.29	Jul. 29th, 2003	Project Code Assigner: Wen-kun Yang
6-4	pscreport.ppt	Jul. 30th, 2003	File Author: Bob Chen
6-5	20030801.doc 2006.6.26	Aug. 1st, 2003	Chairman: Wen-kun Yang Recorder: Bob Chen Participants: David、Eva、Yatzu、Ben、Alex Chen、Jalex Alex Copy Receiver: Eddy Mo、Yao Hung、David Lin、Liching Huang
6-6	MEETING MINUTES OF 300MM W.DOC 2003.8.8	Aug. 8th, 2003	Participants: WK, Yao, Ben, Jalex
6-7	300MM WAFER HANDLING CASE.DOC 2003.9.22	Sep. 22nd, 2003	File Author: Wen-kun Yang
6-8	300MM WAFER FOR WL-CSP PRO.XLS 2003.9.29	Sep. 29th, 2003	
7-1	12TO8_A_FT.DOC 2003.10.6	Oct. 3rd, 2003	
	12轉8 SIMULATION.PPT 2003.10.9	Oct. 9th, 2003	File Author: National Tsing Hua University
7-2	300MM WAFER FOR WL-CSP TRI.XLS	Oct. 16th-17th, 2003	Leader: David Lin、David Wang、Ben Lin
7-3	12.DOC 2003.10.29	Oct. 29th, 2003	File Author: Wen-kun Yang
7-4	WAFER LEVEL PACKAGING.PPT 200310.31	Oct. 31st, 2003	File Author: Wen-kun Yang
7-5	RDMEETING MINUTES ON 1106.DOC 2003.11.7	Nov. 7th, 2003	File Author: Wen-kun Yang
8	掃瞄0004.JPG 2003.11.21		Photographer: David Wang
	SCAN0005.JPG、BY003 PSC 013UM 256M	Nov. 21st, 2003	Photographer: David Wang
9-1	921121.JPG	Nov. 21st, 2003	News Paper: Commercial Times
9-2	PRODUCT.DOC 2003.11.21		File Author: Eddy Mo
10-1	ENHANCED WLCSP_APIA.PDF Wafer Level Technology_ACET.ppt	Dec. 4th, 2003	File Author: Wen-kun Yang
10-2	IC Packaging.ppt 2004.3.14		File Author: Wen-kun Yang
10-3	YIELD ANALYSIS OF LOT_61_63.DOC 2004.3.31	Mar. 31st, 2004	Analyst: David Wang
11	TwinMOS出貨單.pdf 2006.6.27	Apr. 21st, 2004	Client: TwinMOS (勤茂資通)

Doc No	File (File Date)	Date	Testimony of Custodian or Qualified Witness
1	Weekly report ww11_2001.doc 2006.6.23	Mar. 16th, 2001	The Reporter: Willy Liaw
	Weekly report ww14_2001.doc 2006.6.23	Apr. 2nd, 2001	The Reporter: Willy Liaw

FO-WLP – Conception Date

Mar. 16th, 2001

Weekly report WW11 by Willy

Date: 01/03/16

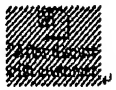
1. Analysis and List the potential MCU/Logic-Mixed Mode Customer.

"MCU customer list.d

2. Visit Prolific(旺玖科技:USB 1394 MCU). Prolific is a potential customer for their new developing devices (USB2.0, 1394) need at least 400Mbps rate, the report.

"Visit Prolific.doc"

3. Analysis the Die size vs PAD vs Pin count of our CSP type for MCU application.



After discuss with customer about our CSP application at MCU/logic-mixed mode devices.

We need to conquer our CSP device Ball count (pin count) limited by die size and the PAD area. If we can solve this weak points for MCU/logic-mixed mode device application, that potential market will be wider...

Size 3mm x 3mm is normal (not small) die size of MCU for 8" wafer (0.35um), and will be shrink again.

Most of the PAD of MCU devices still locate at the die sides(for QFP or SSOP... package type) and occupy a lot of die area. The percentage of these die area occupied by PAD for full die are more and more high for the fab process migration (0.35um> 0.25um>...)

Our CSP processing is avoided to grow Solder Ball at the PAD area currently. This will restrict the pin count that may be necessary for customer application.

Please make a consideration to develop an improvement CSP flow for MCU/Logic mode devices, and re-calculate our CSP process cost.

Ex:

Try to Coat 1 or 2 layers at the PAD area, and can grow ball on the PAD area...

Weekly report WW11 by Willy

Date:90/03/16

1. Analysis and List the potential MCU/Logic-Mixed Mode Customer.


"MCU customer list.d

2. Visit Prolific(旺玖科技:USB 1394 MCU). Prolific is a potential customer for their new developing devices (USB2.0, 1394) need at least 400Mbps rate, the report.


"Visit Prolific.doc"

3. Analysis the Die size vs PAD vs Pin-count of our CSP type for MCU application.


"After discuss with customer

4. Analysis and study the Reliability data for CSP.

Best regards.
Willy

After discuss with customer about our CSP application at MCU/logic-mixed mode devices.

We need to conquer our CSP device Ball count (pin-count) limited by die size and the PAD area. If we can solve this weak points for MCU/logic-mixed mode device application, that potential market will be wider…

Size 3mm x 3mm is normal (not small) die size of MCU for 8" wafer (0.35um), and will be shrink again.
Most of the PAD of MCU devices still locate at the die sides(for QFP or SSOP… package type) and occupy a lot of die area. The percentage of these die area occupied by PAD for full die are more and more high for the fab process migration (0.35um> 0.25um>…)
Our CSP processing is avoided to grow Solder Ball at the PAD area currently. This will restrict the pin-count that may be necessary for customer application.

Please make a consideration to develop an improvement CSP flow for MCU/Logic mode devices, and re-calculate our CSP process cost.
Ex:
Try to Coat 1 or 2 layers at the PAD area, and can grow ball on the PAD area…

Market & Reliability WW14 Report

Date: 04/02/2001
By Willy

1. Updated: Analysis and List the potential MCU/Logic-Mixed Mode Customer.


"MCU customer list.d

2. Visit ELAN(義隆電子, Consumer, Toy, MCU…), the visit report.


"Visit ELAN.doc"

3. Support to Analysis and verify the UV ERASER specification and requirement for Alliance FLASH CP project.

4. Analysis Reliability requirement for CSP, Search and find the MAXIM CSP (FAN-IN type, also without under-fill, applicants at RF, analog, SOC…) reliability requirement data as our Reliability requirement reference.

5. Analysis the possibility for our CSP to applicant at DDR bus terminal/power management market.

Best regards.
Willy

Affidavit of Facts

I, Willy Liaw (廖昱基) , was a Marketing Manger of ACE (Advanced Chip Engineering Inc.) formerly, a company organized under the laws of Taiwan, R.O.C., and having a business address of No.65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu, Taiwan, R.O.C.

In my weekly reports I wrote on March 16, 2001 and April 2, 2001, I brought up WLP demand of market in the reports, and made a description of customer requirement for Fan-out WLP at the conference. I hereby attest that the reports and attachments are true.

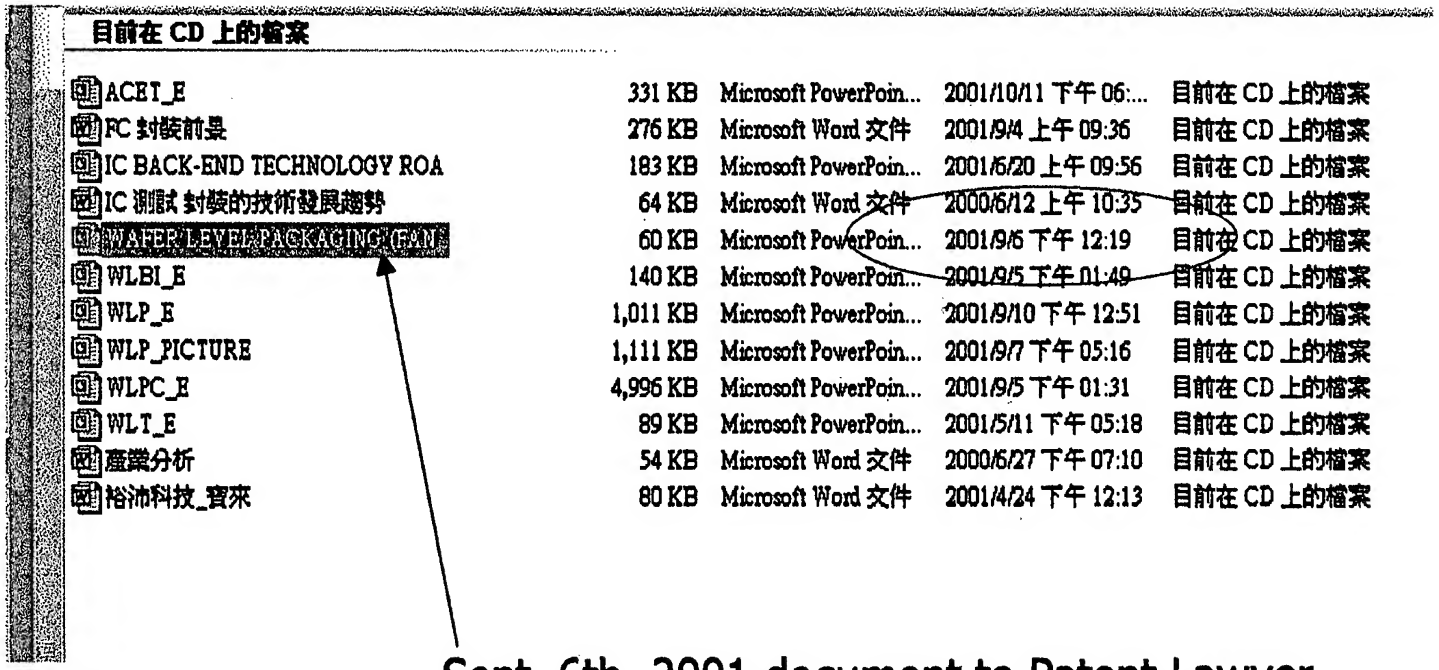
I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature Willy Liaw

Date Sep. 11, 2006.

Doc No	File (File Date)	Date	Testimony of Custodian or Qualified Witness
2	FO-WLP patent document to patent lawyer	Sep. 6th, 2001	

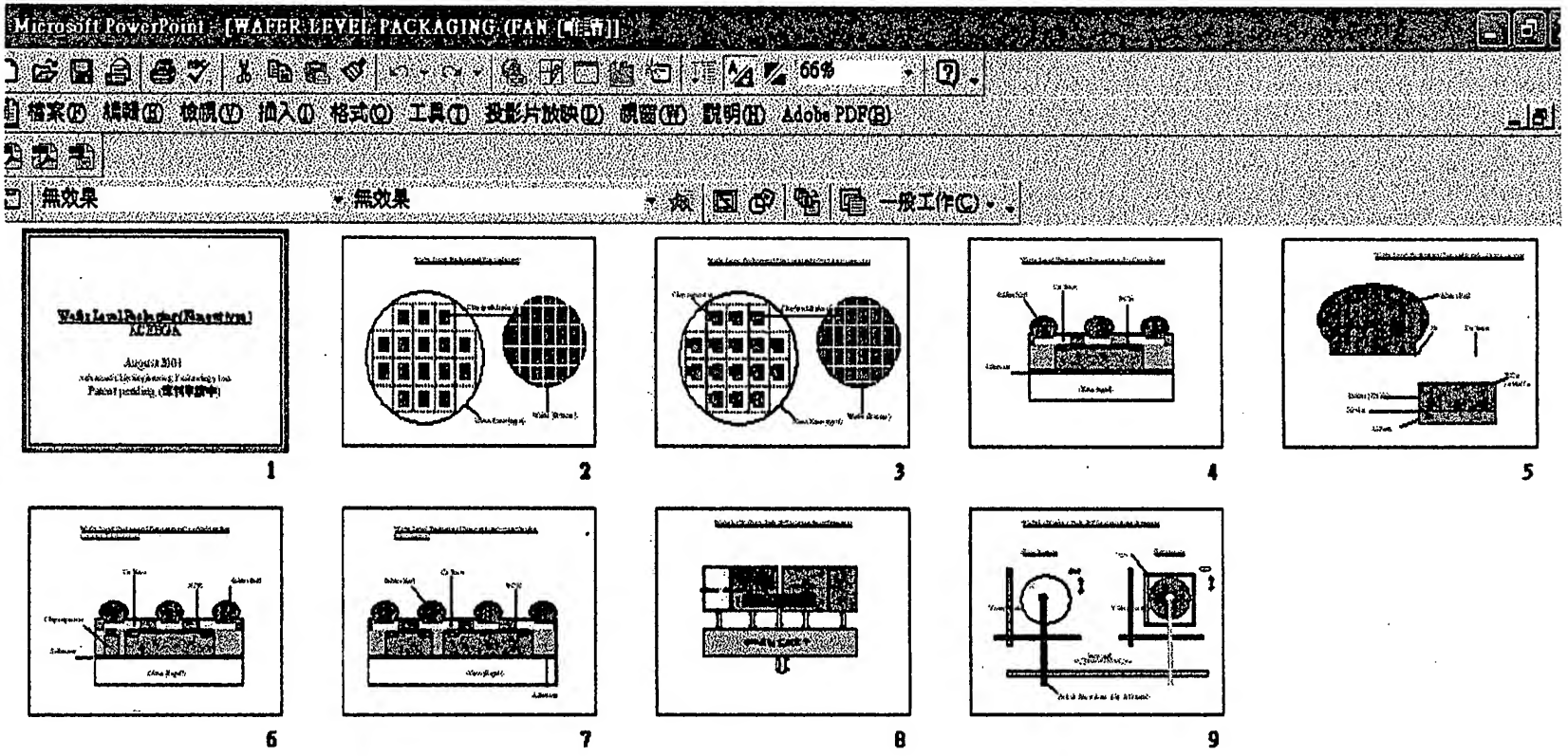
FO-WLP Patent document to Patent lawyer date



Sept. 6th, 2001 document to Patent Lawyer

Doc No	File (File Date)	Date	Testimony of Custodian or Qualified Witness
3	WAFER LEVEL PACKAGING (FAN.PPT) 2001.9.6	Sep. 6th, 2001	File Author: Wen-kun Yang
	FO-WLP patent document to patent lawyer WLP-FAN OUT.XLS 2001.9.2	Sep. 2nd, 2001	File Author: Wen-kun Yang File Receiver: Vincent Chiang
3-1	Official Document of Taiwan IPO (includes the Application and Certificate)	Sep. 25th, 2001	

FO-WLP Patent document contents to Patent lawyer (I)



Wafer Level Packaging (Fan out type)

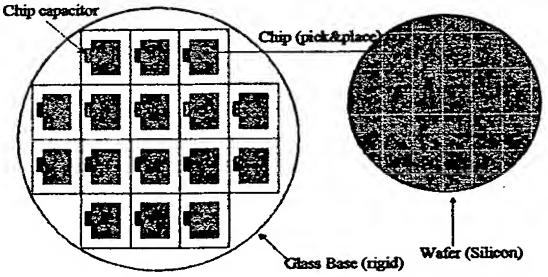
ACEBGA

August 2001

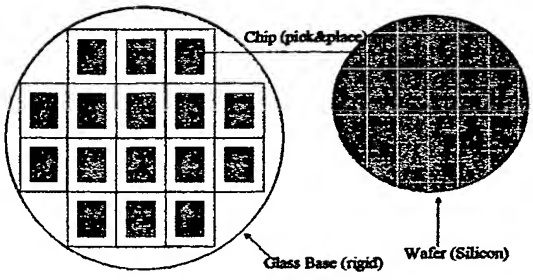
Advanced Chip Engineering Technology Inc.

Patent pending (專利申請中)

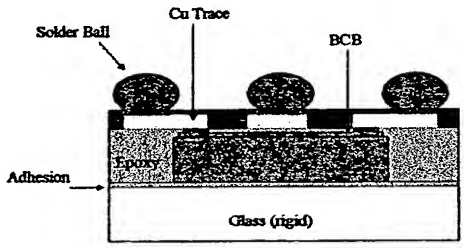
Wafer Level Packaging (Fan out type)w/build-up capacitor



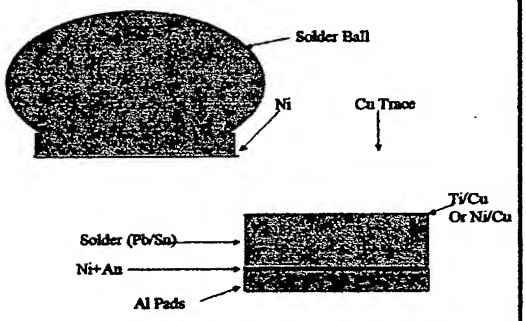
Wafer Level Packaging (Fan out type)



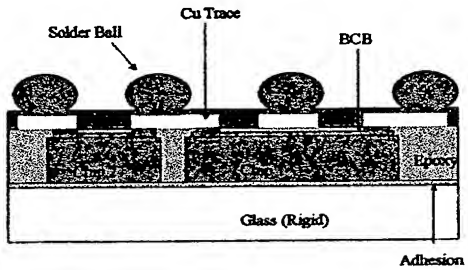
Wafer Level Packaging (Fan out type) - Cross Section



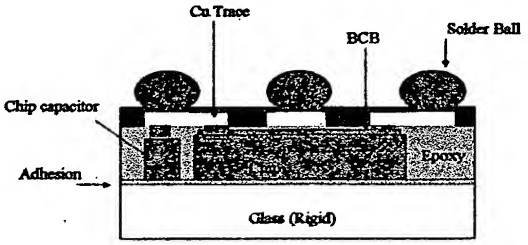
Wafer Level Packaging (Fan out type) - Cross section



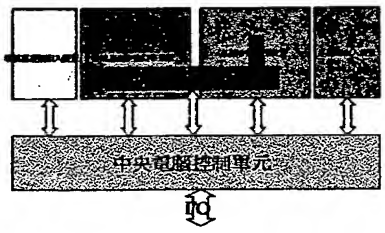
Wafer Level Packaging (Fan out type) - w/multi chips
[Cross Section]

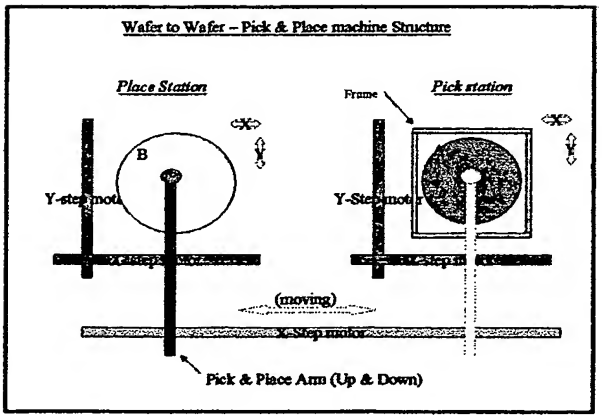


Wafer Level Packaging (Fan out type) – w/build up chip capacitor [Cross Section]



Wafer to Wafer – Pick & Place machine Structure




Wafer to Wafer – Pick & Place machine Structure
Place Station
Pick station
Frame
B
(moving)
Pick & Place Arm (Up & Down)

FO-WLP Patent document contents to Patent lawyer (II)

Confidential

The Process Flow for Wafer Level Packaging (Fan out type)

Sept. 2nd, 2001

Step	function	machine	Re-mark	Materials
1	Plasma etching for wafer surface	RIE		
2	BCB - spin coating	coater	5 - 6u thickness	BCB
3	Al pads open (aligner,exposuer,develop)	mask	切割線漏BCB	
4	Al pads 化鎳 & 化金處理		inter-connect	鎳& 金
Op	Back side grinding	Grinder	wafer thickness 10 - 6 mils	optimal process
5	wafer sawing	sawer		
	12" or 8" glass withthickness 10-15mil			Glass,Ceramic,Silicon
6	adhesion coating on glass surface	coater or 點膠機	thickness ~10u	Epoxy,Acrylic,Phenolic butyral
7	chip pick & place to glass surface	pick & place machine	see drawing(new machine)	
8	curing the adhesion	oven		
9	epoxy coating	coater or printer	10u ~ 25u thickness on top the chip	
10	Au pads open (aligner,exposuer,develop)	mask		
11	curing the epoxy	oven		
12	Plasma etching for wafer surface	RIE or chemical cleaner	Pads treatment	
13	solder printing on the top of Pads	printer	印刷錫Pad用	
14	IR re-flow	IR re-flow	curing solder	
15	Plasma etching for wafer surface	RIE	for inter-connecting	
16	sputter the Ni/Cu or 化鎳	Sputter or plating		
17	PR coating	coater		
18	Cu trace mask (aligner,exposuer,develop)			
19	Cu trace plating	plating machine		
20	Ni plating or 化金			
21	PR remove			
22	etching Ni/Cu			
23	epoxy coating, circuit side	coater	curing	green paint.(epoxy modified)
24	epoxy coating, back side top marking		pre-mark	green paint.(epoxy modified)
25	circuit side solder mask		open solder pads	
26	solder ball placement or printing	printer		
27	IR re-flow		solder curing	
	final testing	tester,prober	using wafer level technology	
28	laser marking	laser marker	post mark process	
29	sawing	sawer	two cut process (epoxy & rigid)	
30	pick & place to tray or T/R		for SMT	tray or tape & Reel

Confidential

Sept. 12th, 2001

The Process Flow for Wafer Level Packaging (Fan out type)

step	function	machine	Re-mark	Materials
1	Plasma etching for wafer surface	RIE		
2	BCB - spin coating	coater	5 - 6u thickness	BCB
3	Al pads open (aligner,exposuer,develop)	mask	切割線無BCB	
4	Al pads 化鎳 & 化金處理		inter-connect	鎳 & 金
Op	Back side grinding	Grinder	wafer thickness 10 - 6 mils	optional process
5	wafer sawing	sawer		
	12" or 8" glass w/thickness 10-15mil			Glass,Cermaic,Silicon
6	adhesion coating on glass surface	coater or 貼膜機	thickness ~10u	Epoxy,Acrylic,Phonolic butyral
7	chip pick & place to glass surface	pick & place machine	see drawing(new machine)	
8	curing the adhesion	oven		
9	epoxy coating	coater or printer	10u ~ 25u thickness on top the chip	
10	Au pads open (aligner,exposuer,develop)	mask		
11	curing the epoxy	oven		
12	Plasma etching for wafer surface	RIE or chemical cleaner	Pads treatment	
13	solder printing on the top of Pads	printer	祇填滿Pad洞	
14	IR re-flow	IR re-flow	curing solder	
15	Plasma etching for wafer surface	RIE	for inter-connecting	
16	sputter the Ni/Cu or 化鎳	Sputter or plating		
17	PR coating	coater		
18	Cu trace mask (aligner,exposuer,develop)			
19	Cu trace plating	plating machine		
20	Ni plating or 化金			
21	PR remove			
22	etching Ni/Cu			
23	epoxy coating, circuit side	coater	curing	green paint (epoxy modified)
24	epoxy coating, back side top marking		pre-mark	green paint (epoxy modified)
25	circuit side solder mask		open solder pads	
26	solder ball placement or printing	printer		
27	IR re-flow		solder curing	
	final testing	tester/prober	using wafer level technology	
28	laser marking	laser marker	post mark process	
29	sawing	sawer	two cut process (epoxy & rigid)	
30	pick & place to tray or T/R		for SMT	tray or tape & Reel

wkyang

Sept. 12th, 2001

The advantage of wafer level packaging by using the fan out type

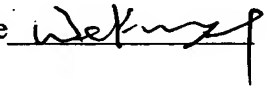
- ✔ Can keep the same ball pitch once die shrink (independ on the die size)
- ✔ Only packaging the good dies (to reduce the cost)
- ✔ Can build up the chip capacitor into the package
- ✔ Can do the multi chip packaging with small size
- ✔ Can do the wafer level final testing to reduce the testing cost
- ✔ Can using the existing tooling for either 8" or 12" wafer set-up
- ✔ Can using the solder as buffer to improve the reliability
- ✔ Can build up the dummy ball to improve the reliability
- ✔ Same ~~TCE~~ CTE between Silicon and Glass (better reliability)
- ✔ Can using the existing equipment of packaging (wafer level packaging)
- ✔ No need the substrate or lead frame
- ✔ Can use the rigid based (glass, ceramic, silicon etc.) to improve the reliability

Affidavit of Facts

I, Wen-kun Yang(楊文焜), am a C.E.O of ACE (Advanced Chip Engineering Technology Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No. 65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu 303, Taiwan, R.O.C.

I hereby attest that, before September 6, 2001, I have created the document of fan-out wafer level packaging and its process flow after discussion with other inventor (Dr. WP Yang). The document including the conception of structure, process flow of fan-out wafer level package, those two files "Wafer Level Packaging (Fan-out type)" and "The process flow for wafer level packaging (Fan-out type)" has been delivered to Mr. Vincent Chiang of Himark Counselors for creating the official document and filing the patent in Taiwan。

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature 

Date Sept. 11, 2006

3 - 1

中華民國專利證書

發明第 一七七七六六 號

發明名稱：晶圓型態擴散型封裝之製程

專利權人：裕沛科技股份有限公司

發明人：楊文焜、楊文彬

專利權期間：自中華民國 九十二 年 五 月 十一 日
至一一〇 年 九 月 二十四 日止

上開發明業經專利權人依專利法之規定取得專利權

經濟部智慧財產局
局長 蔡練生

中華民國 九十五 年 五 日

注意：專利權人未依法繳納年費者，其專利權自原定繳費期限屆滿之次日消滅。

CERTIFICATE OF PATENT, Taiwan, R. O. C.

Certificate No.: 177766

Title of Invention: Fan-Out Wafer Level Packaging

Proprietor(s): Advanced Chip Engineering Technology Inc.

Inventor(s): Wen-Kun Yang, Wen-Ping Yang

Patent Period: May. 11th, 2003 – Sep. 24th, 2021

This is to Certify that, in accordance with the Patent Law, a Patent has been granted to the proprietor(s) for the invention above.

Notice:
In case of the patentee's failure of effecting the payment of a patent annuity in accordance with the Patent Law, the invention patent right shall extinguish from the day following the expiration of the original statutory period for such payment.

Tsai Lien-sheng

Director-General

Intellectual Property Office, MOEA

September 5th, 2003

Amended Date:

Application Date: Sep. 25th, 2001	Serial No.: 90123655
Internal Class: H01L-23/02	

(Column above are filled by Taiwan IPO) Date:

Patent Application 531854

1. Title of Invention	Chinese	晶圓型態擴散型封裝之製程
	English	Fan-Out Wafer Level Packaging
2. Inventors	Name (Chinese)	1. 楊文焜 2. 楊文彬
	Name (English)	1. Wen-Kun Yang 2. Wen-Pin Yang
	Citizenship	1. Taiwan, R.O.C. 2. Taiwan, R.O.C.
	Home Address	1. No.47, Lane 6, Ankang St., Xian Shui Village, Hsinchu City 300, Taiwan (R.O.C.) 2. No.112, Jhulian St., Hsinchu City 300, Taiwan (R.O.C.)
3. Applicants	Name (Appellation) (Chinese)	1. 裕沛科技股份有限公司
	Name (Appellation) (English)	1. Advanced Chip Engineering Technology Inc.
	Citizenship	1. Taiwan, R.O.C.
	Business Address (Firm)	No. 65, Kuang-Fu North Rd., Hsin-Chu Industrial Park HU-KOU,, Hsin-Chu 303, Taiwan, R.O.C
	Name of Applicant's Representative (Chinese)	1. 楊文焜
	Name of Applicant's Representative (English)	1. Wen-Kun Yang

證據一

八、十

年 月 日 修正

申請日期：90.6.25	案號：90123655
類別：H01L-23/62	年 月 日 修正 年 月 日 補充

（以上各欄由本局填註）

發明專利說明書 531854

一、發明名稱	中文	晶圓型態擴散型封裝之製程
	英文	
二、發明人	姓名（中文）	1. 楊文焜 2. 楊文彬
	姓名（英文）	1. 2.
	國籍	1. 中華民國 2. 中華民國
	住、居所	1. 新竹市仙水里18鄰安康街6巷47號 2. 新竹市竹蓮街112號
三、申請人	姓名（名稱）（中文）	1. 裕沛科技股份有限公司
	姓名（名稱）（英文）	1. Advanced Chip Engineering Technology Inc.
	國籍	1. 中華民國
	住、居所（事務所）	1. 新竹縣湖口鄉光復北路65號
	代表人姓名（中文）	1. 楊文焜
	代表人姓名（英文）	1.

四、中文發明摘要 （發明之名稱：晶圓型態擴散型封裝之製程）

本發明是一種半導體封裝技術，特別是有關於利用擴散型（fan out)晶圓型態封裝製程製作封裝之方法。本發明包含切割晶粒後，經過篩選，將晶粒黏著於玻璃底座上，再將黏於晶粒上的金屬墊的I/O接頭透過特殊材質與方式，將I/O接頭植球的位置，以擴散型（fan out)方式，將接觸點往外擴散到晶粒的邊緣甚至晶粒的外圍，此種接觸點往外擴散，由於有較大的範圍來植入I/O植球，因此，一來可以增加I/O植球的數目，增加更多I/O接觸點，二來可以減少由於接觸點距（pitch)過於接近 所造 成的訊號干擾（signal coupling)及銲錫接頭過於接 近時造成的銲錫橋接（solder bridge)問題。本發明的特徵 是延用原來之封裝機台，不需額外花費，同時，本發明可 以應

英文發明摘要 （發明之名稱：）

四、中文發明摘要　(發明之名稱：晶圓型態模散型封裝之製程)

用到8吋與12吋晶圓的封裝過程，又可以包含到晶粒與電容以及多晶粒(multi-chip)或多種 被動元件，例如中央處理器、DRAM, SRAM等等在封裝底座的封裝過程。此外，由於所選用的底做為玻璃底座，不會產生減少不同層之間，由於材質使用的不同所引發的應力不平衡問題，增加其可靠度。

英文發明摘要　(發明之名稱：)

案號 00123655　　年　月　日　　修正

本案已向

國(地區)申請專利	申請日期	案號	主張優先權
無			

有關微生物已寄存於

寄存日期	寄存號碼
無	

五、發明說明 (1)

發明領域：

本發明與一種半導體封裝有關，特別是有關於利用擴散型 (fan out)晶圓型態封裝製程製作封裝之方法。

發明背景：

隨著電子元件尺寸的縮小化後，在積體電路的製造過程上出現許多新挑戰。且由於電腦以及通訊技術之迅勃發展，伴隨需要的是更多不同種類與應用之電子元件。例如，由語音操作之電腦界面或其他通訊之界面均需要許多之記憶元件以及不同類型之半導體元件。是故，積體電路之趨勢仍然會朝向高積集度發展。隨著半導體技術之快速演進，電子產品在輕薄短小、多功能速度快之趨勢的推動下，IC半導體的I/O數目不但越來越多密度亦越來越高，使得封裝元件的引腳數亦隨之越來越多，速度的要求亦越來越快。半導體晶片通常個別地封於塑膠或陶瓷材料之封裝體之內。封裝體之結構必須可以保護晶片以及將晶片操作過程中所產生之熱散出，傳統之封裝亦被用來作為晶片功能測試時之用。

早期之封裝技術主要以導線架為主之封裝技術，利用引腳做為訊號之輸入以及輸出。而在高密度輸入以及輸出端之需求之下，導線架之封裝目前已不符合上述之需求。目前，在上述之需求之下，封裝也越做越小以符合目前之趨勢，而高密度輸出/輸入端 (I/O)之封裝也伴隨球矩陣排

五、發明說明 (2)

列封裝技術（ball grid array;以下簡稱BGA封裝）之發展而有所突破，因此，IC半導體承載的封裝趨向於利用球矩陣排列封裝技術（BGA）。BGA構裝的特點是，負責I/O的引腳為球狀較導線架封裝元件之細長引腳距離短且不易受損變形，其封裝元件之電性的傳輸距離短速度快，可符合目前及未來數位系統速度的需求。例如，於美國專利U. S. Patent No.5629835，由Mahulikar等便提出一種BGA之結構，發明名稱為"METAL BALL GRID ARRAY PACKAGE WITH IMPROVED THERMAL CONDUCTIVITY"。又如美國專利U. S. Patent No. 5,239,198揭露一種封裝形式，此封裝包含一組裝於印刷電路板上之基板，基板利用FR4材質組成，該基板上具有一導電線路形成於基板之一表面。

此外，目前已經有許多不同型態之半導體封裝，不論是哪一種型態之封裝，絕大部分之封裝為先行切割成為個體之後再進行封裝以及測試。而美國專利有揭露一種晶圓型態封裝，請參閱，US5323051，發明名稱為"Semiconductor wafer level package"。此專利在切割晶粒之前先行進行封裝，利用玻璃當作一黏合材質使得元件封於一孔中。一遮蓋之穿孔做為電性連結之通道。因此，晶圓型態封裝為半導體封裝之一種趨勢。另外所知之技術將複數晶粒形成於半導體晶圓之表面，玻璃利用黏著物質貼附於晶圓之表面上。然後，沒有晶粒的那一面將被研磨以降低其厚度，通常稱做背面研磨（back

五、發明說明 (3)

grinding)。接著，晶圓被蝕刻用以分離IC以及暴露部分之黏著物質。

此外，以往之封裝技術領域中，I/O鋁墊部分是接於晶粒的表面，由於晶粒面積有限，I/O鋁墊在該有限面積下，將限制其鋁墊數目。再者，I/O鋁墊之間距過小將會造成訊號間的耦合(signal coupling)或訊號間的干擾。

由於晶圓型態封裝將成為封裝技術之趨勢，本發明的主要特徵是取代以往晶粒表面上I/O植球的位置，以擴散型(fan out)方式，將接觸點往外擴散以提升較大的範圍來植入做為I/O之植球，因此，其優點包含可以增加I/O植球的數目，亦即增加更多I/O，或是在晶粒朝向縮小化之趨勢下，保持I/O之最小間距(pitch)以防止過於接近所造成的訊號干擾(signal coupling)與銲錫接頭過於接近所造成的銲錫橋接(solder bridge)問題。

發明目的及概述：

本發明之目的為提供一晶圓型態擴散型封裝之方法。

本發明之另一目的為提供一種晶圓型態封裝以及其製程。

本發明之晶圓型態封裝製程包含提供，將切割過之晶圓 經過篩選通過品質管制後的晶圓，選取好的晶粒

五、發明說明 (4)

(die)，透過吸取與放置的動作重新排列於一新的玻璃底座。並經由黏著劑(adhesion)將各個晶粒黏著於上述底座上。晶粒擺至於玻璃底座上，使晶粒間的距離(pitch)加大，其目的是希望在後續封裝過程中多出來的空間能夠容納擴散型(fan out)圓錫球陣列(ball array)。此擴散型封裝技術可以提昇I/O數目，或是在晶粒尺寸縮小情形下，仍保持其理想間距(pitch)以防止I/O間之訊號干擾。將進行封裝之晶圓正面(或第一表面)具有做為輸入輸出之金屬墊，例如鋁墊(I/O pad or aluminun pad)，該金屬墊是做為內連線(inter connect)之用，而且是利用光罩(mask)經過校準(alignment)、曝光與顯影(developer)過程形成於晶圓的上面。先行在晶圓與鋁墊的上面透過旋轉塗佈機(spin coater)旋塗(spin coating)一層BCB絕緣層。接著，去除部分的BCB，形成第一開口(opening)以曝露出下方的金屬鋁墊。接著，於鋁墊表面形成一化鎳/化金(Ni/Au)膜層。接著，再將晶圓切割以形成個別之晶粒單體。接著，將上述之晶粒經由篩選與品質檢驗合格後經由具有吸附與放置功能的機械將晶粒配置於玻璃底座上面以黏著物固定，並予以固化。

接著，全面性地填充一層第一環氧樹脂(EPOXY)於玻璃底座、晶粒、BCB與開口的鋁墊的上面。然後，經過光阻型蝕刻或化學藥劑以移除鋁墊上方的第一環氧樹脂，形成第二開口暴露鋁墊。接著，在爐(oven)內予以固化此第一環氧樹脂。接著，用銲錫(solder)以網印(printer)技

五、發明說明 (5)

術填滿該第二開口。

然後，再上一層鈦/銅(Ti/Cu)於銲錫(solder)的上面。接著，在鈦/銅層上面以朝外擴散(fan out)的方式，電鍍(plating)一定面積的銅導線，銅導線的位置，一端是與鋁墊切齊，另一端以水平向方向朝外擴散(fan out)的方式牽引導線。在定義銅導線之光阻去除前，先電鍍一化鎳或化金，之後去除光阻。然後蝕刻鈦/銅。接著，全面性地塗佈(coating)一層第二環氧樹脂(epoxy)於銅導線與下層環氧樹脂的上面，並以固化之步驟利用紫外線照射或加熱處理以硬化上述之第二環氧樹脂。

然後，去除銅導線上面的部分第二環氧樹脂(epoxy)並形成第三開口，其位置儘可能位於銅導線的外側(遠離鋁墊的一邊)以利於製作擴散型(fan out)I/O結構。接下來的步驟是，在第三開口上面形成一層鎳(Ni)層，接著在第三開口處，鎳(Ni)層的上面，透過網印技術或植球技術，植入焊錫球(solder ball)，焊錫球經過此一封裝過程設計後的位置，並不在金屬墊的正上方，而是水平向側沿伸到金屬墊的側邊上。最後，完成切割晶粒與底座玻璃的步驟。

本發明之結構如下：

一種晶圓型態擴散型封裝包含：絕緣基座；晶粒配置於該絕緣基座之上，其中晶圓包含複數個鋁墊形成於其上；BCB層，塗佈於晶粒表面，並具有複數第一開口暴露

五、發明說明 (6)

複數鋁墊；銲錫填充於第一開口；第一環氧樹脂，塗佈於晶粒、絕緣基座以及BCB層之上；銅導線配置於第一環氧樹脂並與銲錫連接；第二環氧樹脂塗佈於銅導線之上並具有第二開口暴露部分之銅導線；錫球配置於第二環氧樹脂之上並填入該第二開口與該銅導線連接。

其中更包含銅種子層形成於第一銲錫之上，銅種子層包含鈦/銅(Ti/Cu)或鎳/銅(Ni/Cu)。其中更包含阻障或黏著層形成於鋁墊之上，阻障或黏著層之材質組成包含鎳/金(Ni/Au)。而錫球與該銅導線之介面包含鎳(Ni)。本發明將上述結構之封裝稱為ACE BGA。

發明詳細說明：

本發明揭露一種晶圓型態封裝(wafer level packaging, WLP)以及製作晶圓型態封裝之方法，詳細說明如下，所述之較佳實施例只做一說明非用以限定本發明，首先參閱圖一，將經過測試以及切割過之晶圓經過篩選通過品質管制後 的晶粒，選 取測試 合格之晶粒(die)1a，透過吸取與放置裝置將其重新排列配置於一新的玻璃底座1(該底座可以是玻璃、陶瓷或矽晶)，並經由黏著劑(adhesion)將各個晶粒黏著於上述底座1上，該黏著劑厚度大約10μm，該固化黏著劑的過程是利用旋塗機(spin coater)進行黏著動作。晶粒擺至於玻璃底座上，晶粒間

五、發明說明 (7)

的距離(pitch)加大，其目的是希望在後續封裝過程中具有充足之空間能夠容納擴散型(fan out)圓錫球陣列(ball array)。此擴散型封裝技術可以提昇I/O數目，或是在晶粒尺寸縮小情形下，仍保持其理想間距(pitch)以防止I/O間之訊號干擾。封裝的大小面積取決於後續製程完成後擴散型(fan out)圓錫球陣列(ball array)之間的間距(pitch)大小而定。在另一實施例中，該玻璃基座1上也可以包含電容(capacitor)1b配置於晶粒之側，以提升濾波效果，如圖二所示。

以下所述封裝過程是從具有金屬墊(metal pad)的單一晶粒開始其封裝過程：

圖三中，將進行封裝之晶圓2正面(或第一表面)具有做為輸入輸出之金屬墊，例如鋁墊(I/O pad or aluminum pad)4，該金屬墊是做為內連線(inter connect)之用，利用光罩(mask)經過校準(alignment)、曝光與顯影(developer)過程，將金屬墊形成於晶粒的上面。接著，在晶圓上透過旋轉塗佈機(spin coater)旋塗(spin coating)一層BCB絕緣層8於晶粒2與鋁墊4的上面以保護晶粒，BCB的厚度大約為5-10μm。

接著，經過光罩(mask)校準(alignment)、曝光與顯影(developer)過程以去除部分的BCB 8，形成第一開口(opening)9以曝露出下方的金屬鋁墊4，值得注意的是，此切割道(scribe line)上亦被暴露且大於其切割道之寬

五、發明說明 (8)

度，以利於切割時不損及BCB，如圖四所示。之後以電鍍方式形成化鎳或化金11於鋁墊4之上。

經過切割，如圖五表示，將複數個晶粒2a(此處晶圓業經切割形成晶粒)經自篩選與品質檢驗合格後經由具有吸附與放置功能的機械將晶粒2a擺置於玻璃底座6上面，並透過黏著劑7黏著於玻璃底座6上面，接著在爐(oven)內予以固化(curing)。

接著，全面性地在玻璃底座6、晶粒2a、BCB 8與開口的鋁墊4的上面全面性地填充一層第一環氧樹脂(EPOXY)10。接著，如圖六至圖七所示，經過光阻型蝕刻或化學藥劑以移除鋁墊4上方的第一環氧樹脂10，形成第二開口13，並曝露出下方的鋁墊4。接著，在爐(oven)內予以固化，此第一環氧樹脂10，其厚度大約為10-25μm之間(這裡的厚度指的是在晶粒表面上的厚度)。

接著，接著將剩餘的環氧樹脂，以RIE電漿清潔晶粒2a表面。至於上述的剩餘的環氧樹脂則以10表示。上述之鎳/金(Ni/Au)或化鎳層11可做為阻障層或是黏著層之功用。

接著，在鎳/金(Ni/Au)或化鎳層11上方的第二開口13內利用銲錫(solder)12以網印(printer)技術填滿該第二開口13。接著，以紅外線(IR)迴流(reflow)固化(curing)此銲錫(solder)12，然後，全面性地濺鍍一層鈦/銅(Ti/Cu)19於剩餘的環氧樹脂10與銲錫(solder)12的上面，以作為銅種子層(seeding layer)，如圖八所示。

五、發明說明 (9)

接著，如圖九所示，以光阻（未圖示）定義銅導線圖案，利用電鍍方式形成銅導線於鈦/銅（Ti/Cu）19的上面，一端對準第二開口銲錫12的內端（晶粒的內側邊），而另一端以水平向方向朝外擴散（fan out）的方式（晶粒的內側邊），明確的講，也就是說銅導線14的位置，一端是與鋁墊4切齊，另一端以水平向方向朝外擴散（fan out）來牽引導線，其與下層環氧樹脂10及銲錫12的接觸面積較鋁墊4的開口來的大，其目的主要是用來增加I/O的植球區域面積，接著，在銅導線14上面形成一層化鎳（Ni）層或化金層17以做為後續銲錫植球的黏著層，再移除光阻。並移除曝露於剩餘環氧樹脂10的上面部分鈦/銅（Ti/Cu）19。

接著，如圖十所示，全面性地塗佈（coating）一層第二環氧樹脂（epoxy）16於銅導線14、鎳（Ni）層17與下層環氧樹脂10的上面，並以固化之步驟利用紫外線照射或加熱處理以硬化上述之第二環氧樹脂（epoxy），防止銅導線14被氧化。

接著，如圖十一所示，去除銅導線14與鎳（Ni）層17上面的部分第二環氧樹脂（epoxy）16並形成第三開口15，該第三開口15的位置是在銅導線14與鎳（Ni）層17的上面，且儘可能位於銅導線14的外側（遠離鋁墊4的一邊）以利於製作擴散型（fan out）I/O結構。

接著，如圖十二所示，接著在第三開口15處，鎳（Ni）層17的上面，透過網印技術或植球技術植入焊錫球（solder ball）18，由圖中明顯可見，焊錫球18經過此一

五、發明說明 (10)

封裝過程設計後的位置，並不在金屬墊4的正上方，而是水平向側伸到金屬墊4的側邊上。

接著，如圖十三所示，再經過紅外線(IR)迴流(reflow)烘烤(curing)環氧樹脂，晶圓再傳送至晶圓型態測試裝置中進行晶圓型態測試，例如最後測試(final testing)以及切割(sawer)過程，並切割晶粒與晶粒間切割線(scribe line)20與玻璃基座6，以分離個別之封裝體。

本發明之製程較先前技術簡單，在未分割前以晶圓型態進行測試，且在測試後可以沿著切割道切割成個別之晶粒，以吸取放置裝置被置於玻璃基板之上完成晶圓型態擴散型封裝(wafer level fan out packaging)。

圖十四所示，為鎳/金(Ni/Au)或化鎳層11、鈦/銅(Ti/Cu)或鎳/銅(Ni/Cu)19、鎳(Ni)層17各黏著層(glue layer)與阻障層，在內連線的各個位置示意圖。

圖十五所示，為單一晶粒的晶圓型態擴散型封裝(wafer level fan out packaging)成型的剖面圖。本發明也能將晶粒電容2b納入封裝過程，圖十六所示，即為電容2b植入到玻璃基座上與單一晶粒的晶圓型態擴散型封裝(wafer level fan out packaging)的成型剖面圖。在另一實施例中，本發明也能將多晶粒(multi-chip)或多種被動元件整合納入封裝過程，圖十七所示，即為多晶粒(multi-chip)的封裝過程中晶圓型態擴散型封裝(wafer level fan out packaging)的剖面圖，圖中2a、2c即代表不同之晶粒，此種封裝方式可將多晶粒與多種被動元件整合封裝，形成系

五、發明說明 (11)

統式封裝 (system in package)。

本發明的主要特徵是植基於晶圓型態封裝，並使用擴散型 (fan out)方式將晶粒表面上 I/O植球的位置側向延伸，其優點可以增加 I/O植球的數目；可以減少由於接觸點距 (pitch)過於接近所造成的訊號干擾問題。

本發明的主要優點如下：

1.如圖一所示，本發明之晶圓型態封裝之成本較傳統技術低，再藉由已測試及切割過之晶圓經過篩選，將通過品質管制後的晶粒，選取好的晶粒 (die)，透過吸取與放置的動作重新排列於一新的玻璃底座，可以減少製作成本完成擴散型封裝。

2.由於尺寸縮小原則，晶粒 (chip)亦隨之縮小，而為了使得晶粒間的距離 (pitch)仍然保持理想的距離 (以不影響到訊號傳遞耦合為原則)，在本發明中是以晶圓型態擴散型封裝 (wafer level fan out packaging)，將 I/O線向外擴散，並將連線拉到晶粒外的區域，以增加銲錫圓球的數目及維持理想晶粒間的距離 (pitch)。

3.本發明可以應用到 8吋與 12吋晶圓的封裝過程。

4.本發明可以整合晶粒與電容於同一封裝單體。

5.本發明能將多晶粒 (multi-chip)或多種被動元件整合於同一單體，例如中央處理器、DRAM, SRAM等等在封裝底座的封裝過程。

6.本發明能將環氧樹脂中之銲錫當作緩衝區 (buffer zone)，在後續製程中，減少不同層之間，由於材質使用

五、發明說明 (12)

的不同所引發的應力不平衡問題，增加其可靠度(reliability)。

7.本發明的底座是玻璃，其材質與晶粒底材相同，由於材質中均含有矽材質，兩者具有同樣的熱力膨脹係數(thermal coefficient of expansion, TCE)，不會產生應力不平衡現象。

8.本發明的底座可以使用玻璃、灰石與矽晶(glass, ceramic, silicon)以改善其可靠度。

9.本發明的封裝機械部是以現有機械設備進行封裝，可以省去額外添購的費用。

10.本發明可以增加銲錫圓球的數目，其中有些銲錫圓球當作樣本假輸出輸入端(dummy ball)，此dummy ball雖無訊號傳遞之功能卻可供作緩衝區(buffer zone)以減弱不同材質間的應力，減少封裝時晶粒龜裂的現象發生。

本發明以較佳實施例說明如上，而熟悉此領域技藝者，在不脫離本發明之精神範圍內，當可作些許更動潤飾，其專利保護範圍更當視後附之申請專利範圍及其等同領域而定。

圖式簡單說明

圖式簡單說明：

本發明的較佳實施例將於往後之說明文字中輔以下列圖形做更詳細的闡述：

圖一為晶圓級封裝單一晶粒由晶圓切割後厚擺置於玻璃底座之示意圖。

圖二為晶圓級封裝具有電容的晶粒由晶圓切割後擺置於玻璃底座之示意圖。

圖三所顯示為本發明中具有金屬墊的晶粒的表面上形成一層 BCB保護層之示意圖。

圖四所顯示為本發明中去除部分 BCB保護層之示意圖。

圖五所顯示為本發明中，晶粒經過吸附與放置後黏至於底座之示意圖。

圖六所顯示為本發明中，全面性地填充一層第一環氧樹脂之示意圖。

圖七所顯示為本發明中，經過光阻型蝕刻或化學藥劑以移除鋁墊上方的第一環氧樹脂之示意圖。

圖八所顯示為本發明中，用銲錫（solder）以網印（printer）技術填滿該第二開口之示意圖。

圖九所顯示為本發明中，顯示為透過校準、曝光與顯影電鍍（plating）一定面積的銅導線之示意圖。。

圖十所顯示為本發明中，為全面性地塗佈（coating）一層第二環氧樹脂（epoxy）之示意圖。

圖十一所顯示為本發明中，去除銅導線上面的部分第二環

圖式簡單說明

氧樹脂（epoxy）16並形成第三開口之示意圖。

圖十二所顯示為透過網印技術或植球技術，植入焊錫球之示意圖。

圖十三所顯示為切割晶粒與晶粒間切割線與玻璃基座之示意圖。

圖十四所顯示為晶粒上各阻障層的相關位置示意圖。

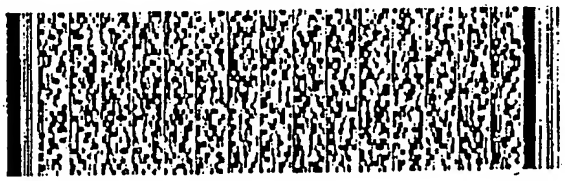
圖十五所顯示為單一晶粒的晶圓型態擴散型封裝成型的剖面圖。

圖十六所顯示為電容植入到玻璃基座上與單一晶粒的晶圓型態擴散型封裝的成型剖面圖。

圖十七所顯示為為多晶粒的封裝過程中晶圓型態擴散型封裝的剖面圖

元件符號對照

晶粒	1a
電容	1b
晶圓	2
晶粒	2a
電容	2b
晶粒	2c
鋁墊	4
玻璃底座	6
黏著劑	7
BCB絕緣層	8



圖式簡單說明

環氧樹脂　10

剩餘的環氧樹脂 10'

化鎳 /化金　11

銲錫　12

第二開口　13

銅導線　14

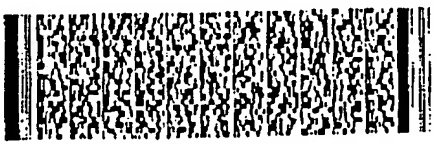
環氧樹脂　16

鎳層　17

焊錫球　18

鈦 /銅　19

晶粒間切割線　20



六、申請專利範圍

申請專利範圍：

1.一種晶圓型態擴散型封裝之製程，該晶圓型態擴散型封裝之製程包含：

提供具有複數晶粒形成於其上之晶圓；

測試該晶圓上之複數晶粒並標記合格之晶粒；

旋塗BCB絕緣層以保護該晶粒；

去除部分的該BCB層，形成第一開口以曝露出該晶粒上之金屬鋁墊；

切割該晶圓以分離該複數晶粒；

經篩選通過品質管制後的晶粒，透過吸取與放置的動作重新排列配置黏著於一絕緣底座之上；

全面性地填充一層第一環氧樹脂於該絕緣底座、該晶粒、該BCB與該第一開口的該鋁墊上；

蝕刻以移除該鋁墊上方的該第一環氧樹脂，形成第二開口；

固化該第一環氧樹脂；

濺鍍一阻障層於該該鋁墊的上；

以網印(printer)技術用銲錫在該阻障層上並填滿該第二開口；

形成銅種子層於銲錫及第一環氧樹脂之上；

利用一光阻電鍍一定面積的銅導線於該銲錫與該阻障層之上；

形成化鎳或化金於銅導線之上；

六、申請專利範圍

去除光阻；

全面性地塗佈（coating）一層第二環氧樹脂（epoxy）於該銅導線之上；

固化上述之該第二環氧樹脂；

去除該銅導線上部分該第二環氧樹脂並形成第三開口；

植入焊錫球於該第三開口；以及

切割該絕緣基座用以分離個別封裝單體。

2.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，其中在形成上述銅導線之前更包含濺鍍一銅種子層於該銲錫與該第一環氧樹脂上面。

3.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，其中該黏著晶粒於該底座的過程，更包含在爐內予以固化該黏著劑。

4.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，其中該BCB絕緣層之厚度大約為5-25μm。

5.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，其中該蝕刻該第一環氧樹脂，以形成該第二開口的過程，是藉由光阻型蝕刻或化學藥劑進行。

6.如申請專利範圍第5項之晶圓型態擴散型封裝之製程，

六、申請專利範圍

其中形成上述第二開口之後，更包含以RIE電漿清洗晶粒表面。

7.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，該阻障層之材料包含鎳/銅或化鎳層。

8.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，完成上述網印(printer)技術後，更包含以紅外線(IR)迴流固化該銲錫。

9.如申請專利範圍第2項之晶圓型態擴散型封裝之製程，其中上述之銅種子層包含鈦/銅。

10.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，其中固化該第二環氧樹脂之步驟係包含利用紫外線照射或加熱處理。

11.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，其中上述植入於該第三開口的之焊錫球係採用網印技術或植球技術。

12.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，其中更包含電容配置於該晶粒之側並排於該玻璃底座上。

六、申請專利範圍

13.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，其中更包含另一晶粒配置於該晶粒之側並排於該玻璃底座上，形成多晶粒(multi-chip)封裝結構，該另一晶粒包含但不限於CPU, DRAM, SRAM等元件。

14.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，其中上述絕緣底座包含玻璃。

15.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，其中上述絕緣底座包含陶瓷。

16.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，其中上述絕緣底座包含矽晶。

17.一種晶圓型態擴散型封裝，包含：
絕緣基座；
晶粒，配置於該絕緣基座之上，其中該晶圓包含複數個鋁墊形成於其上；
BCB層，塗佈於該晶粒表面，並具有複數第一開口暴露該複數鋁墊；
銲錫，填充於該第一開口；
第一環氧樹脂，塗佈於該晶粒、該絕緣基座以及該BCB層之上；
銅導線，配置於該第一環氧樹脂並與該銲錫連接；

六、申請專利範圍

第二環氧樹脂，塗佈於該銅導線之上，並具有第二開口暴露部分之該銅導線；及

錫球，配置於該第二環氧樹脂之上並填入該第二開口與該銅導線連接。

18.如申請專利範圍第17項之晶圓型態擴散型封裝，其中更包含銅種子層形成於該第一銲錫之上。

19.如申請專利範圍第18項之晶圓型態擴散型封裝，其中上述銅種子層包含鈦/銅（Ti/Cu）。

20.如申請專利範圍第18項之晶圓型態擴散型封裝，其中上述銅種子層包含鎳/銅（Ni/Cu）。

21.如申請專利範圍第17項之晶圓型態擴散型封裝，其中更包含阻障或黏著層形成於該鋁墊之上。

22.如申請專利範圍第21項之晶圓型態擴散型封裝，其中該阻障或黏著層包含鎳/鋁（Ni/Al）。

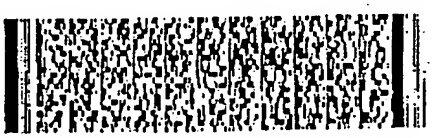
23.如申請專利範圍第17項之晶圓型態擴散型封裝，其中該錫球與該銅導線之介面包含鎳（Ni）。

24.如申請專利範圍第17項之晶圓型態擴散型封裝，其中

六、申請專利範圍

更包含一電容配置於該晶粒之側。

25.如申請專利範圍第17項之晶圓型態擴散型封裝，其中更包含另一晶粒配置於該晶粒之側。



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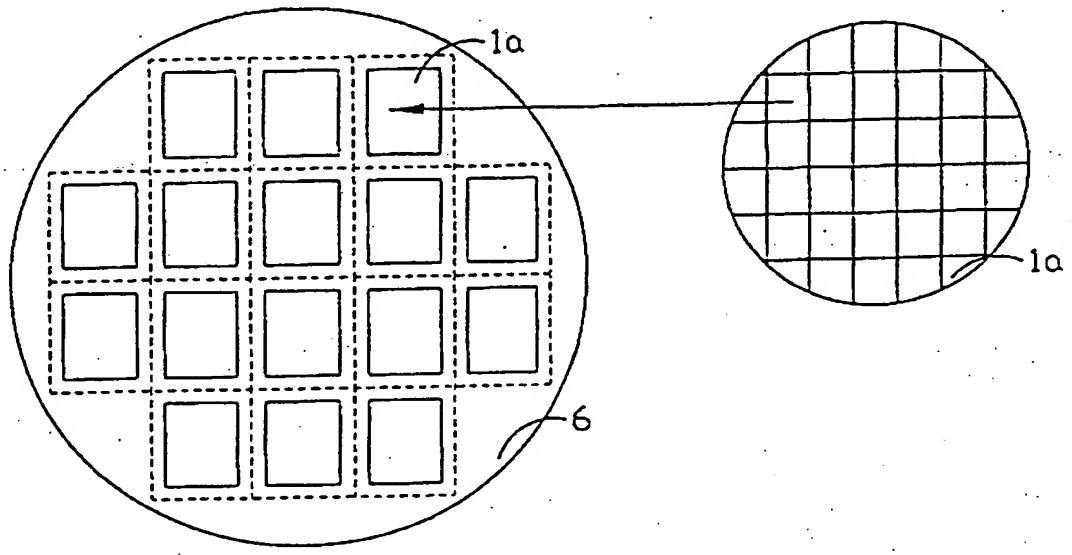
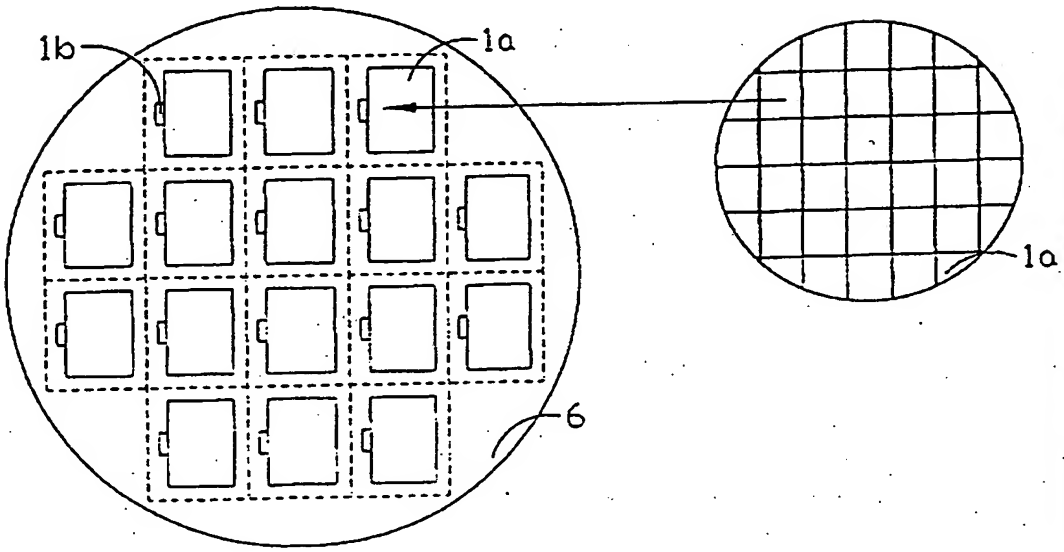
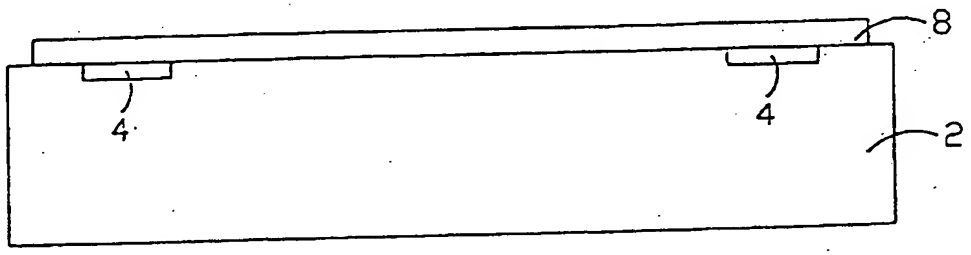


圖一



圖二

圖式



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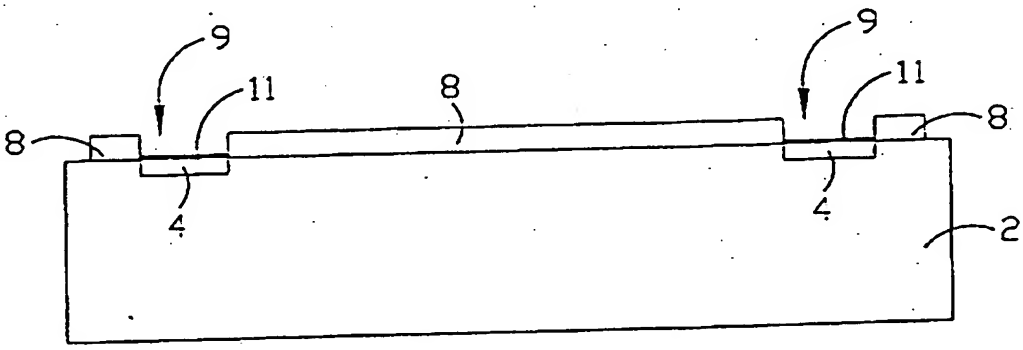

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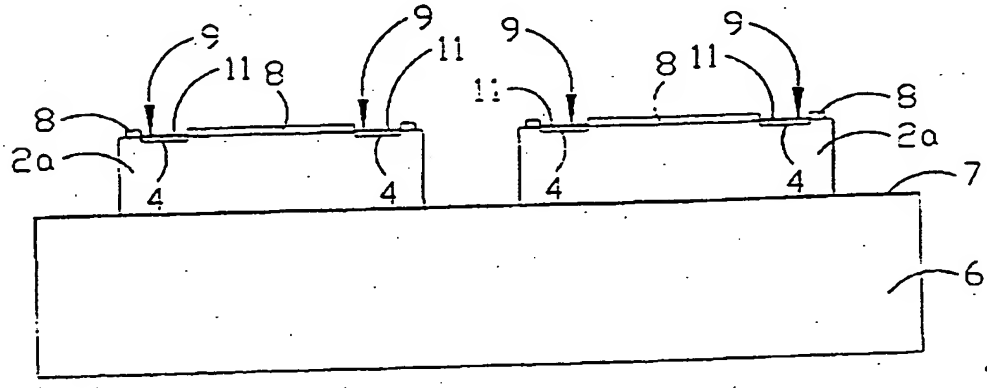

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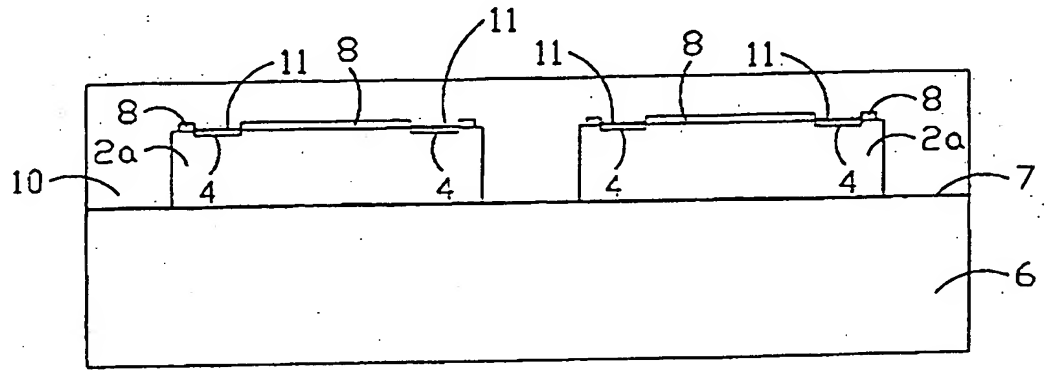
圖式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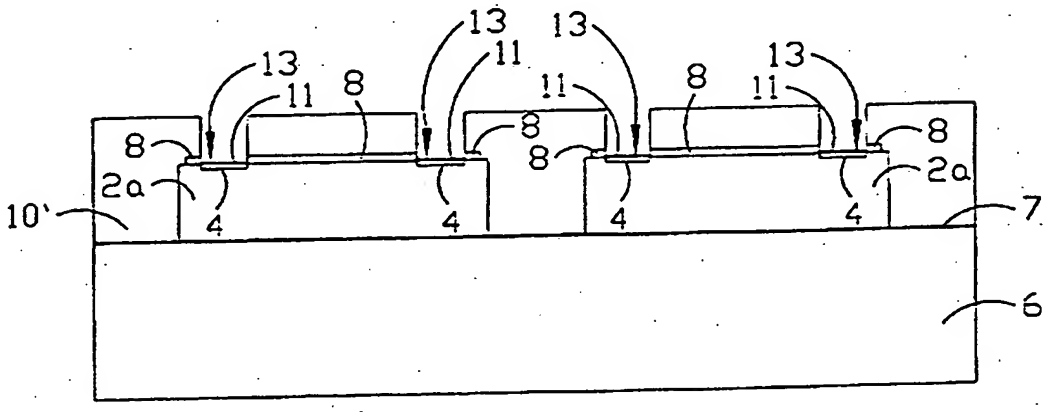
圖六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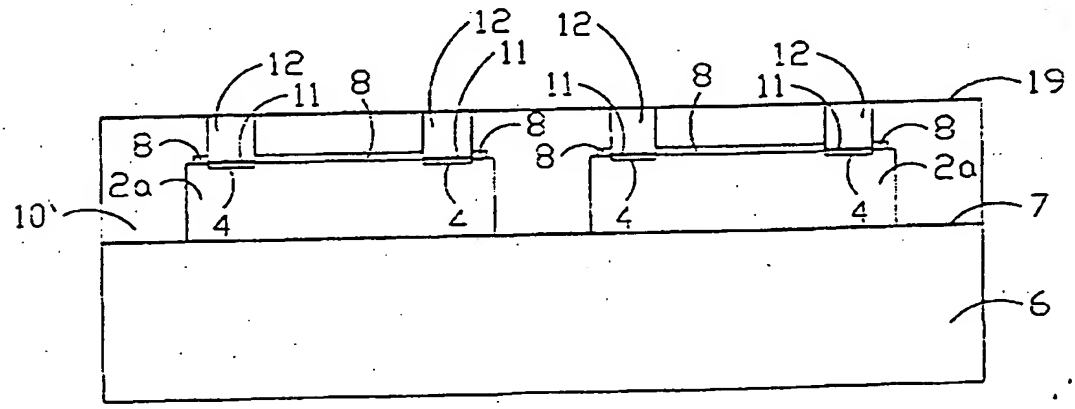
圖七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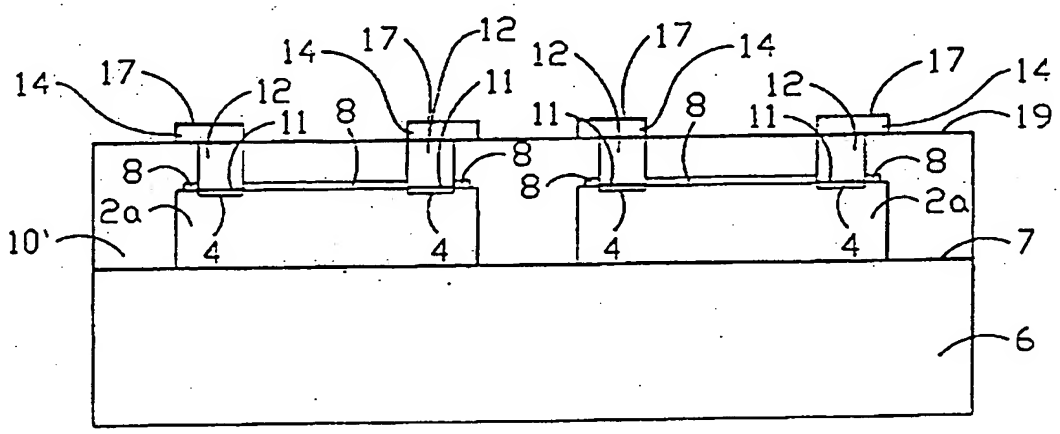
圖八

圖式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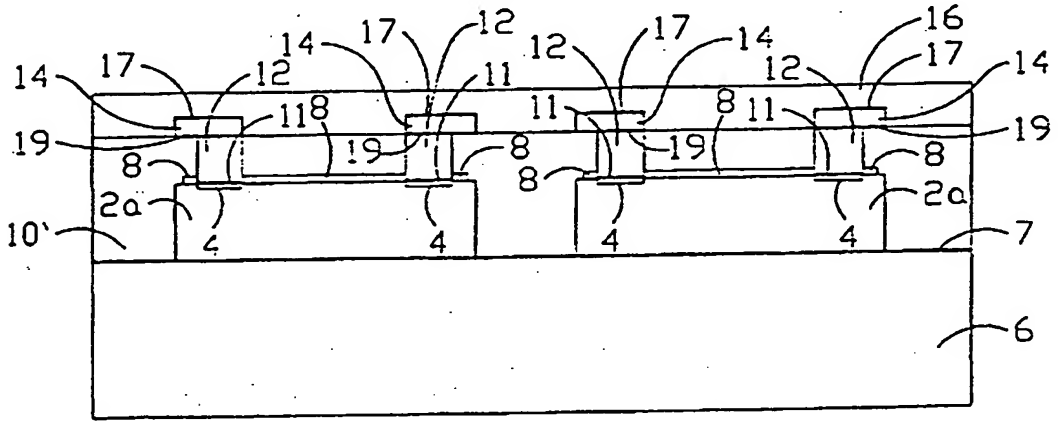
圖九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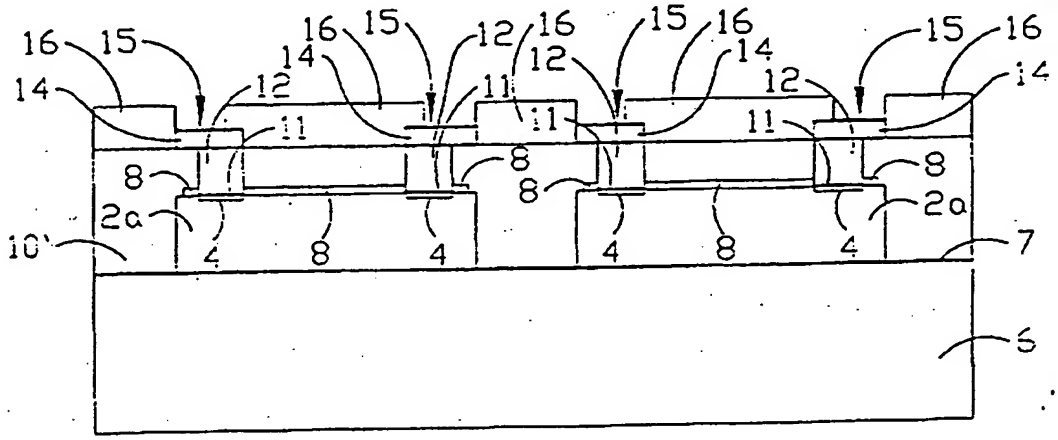
圖十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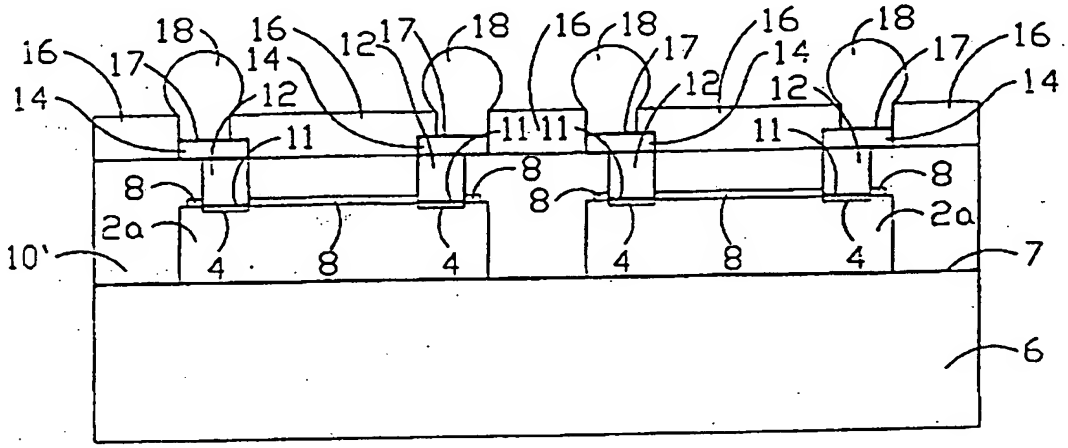
圖十一

圖式



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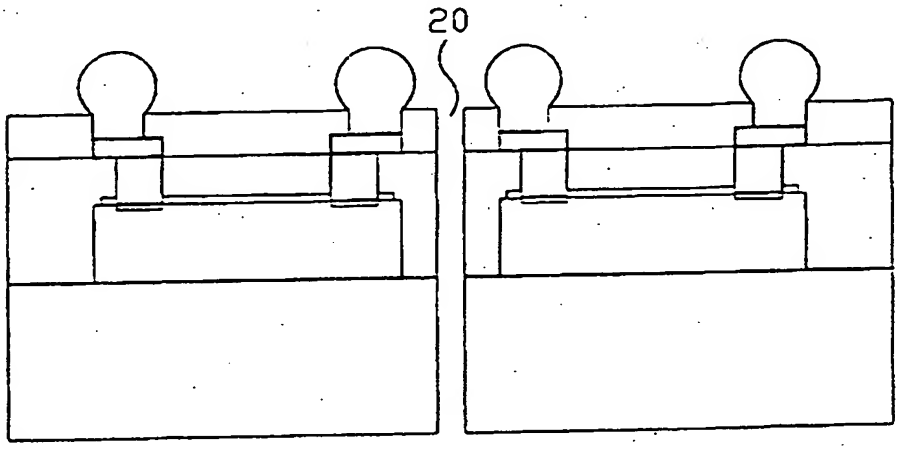

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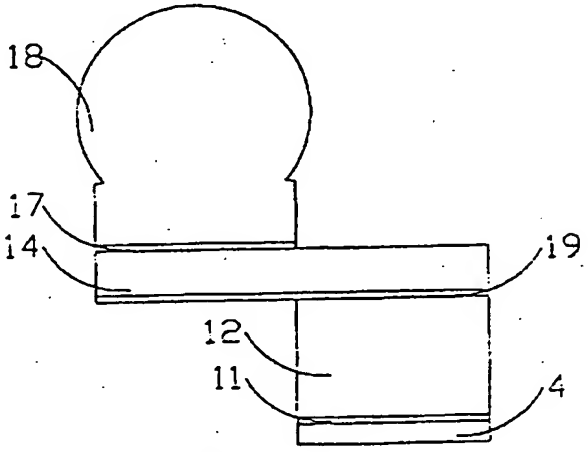

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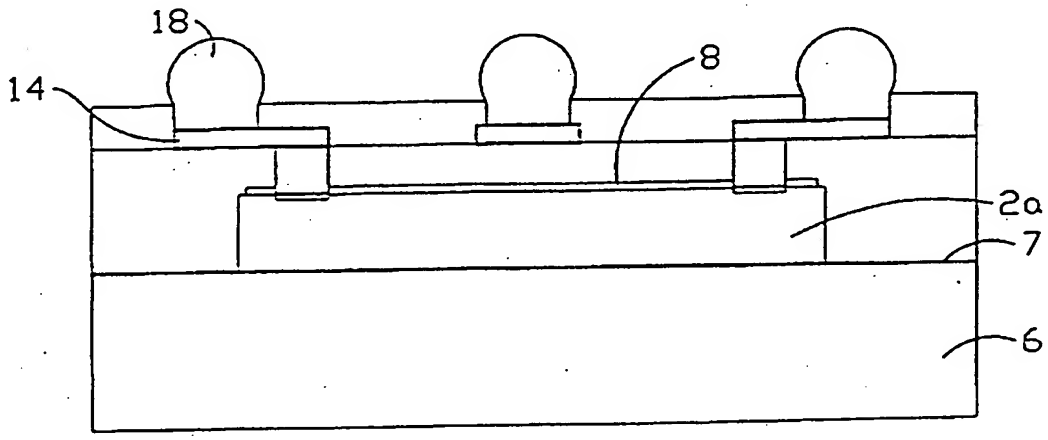
圖式



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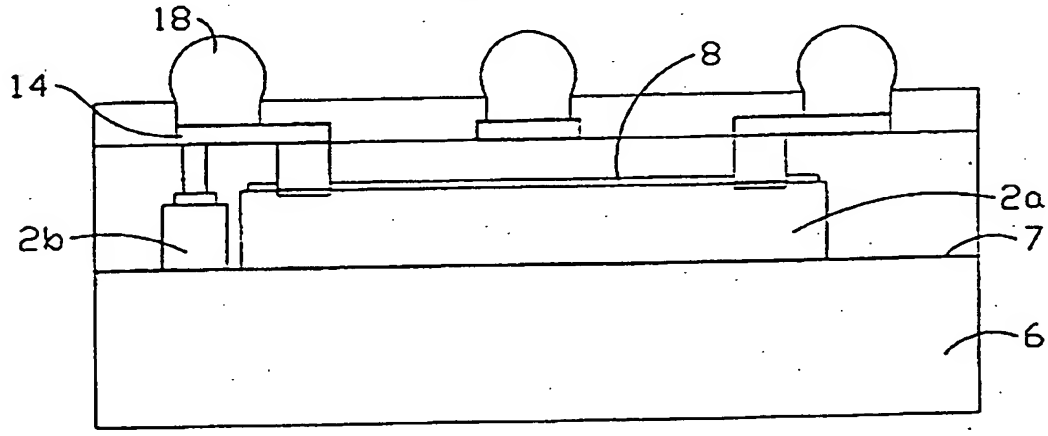

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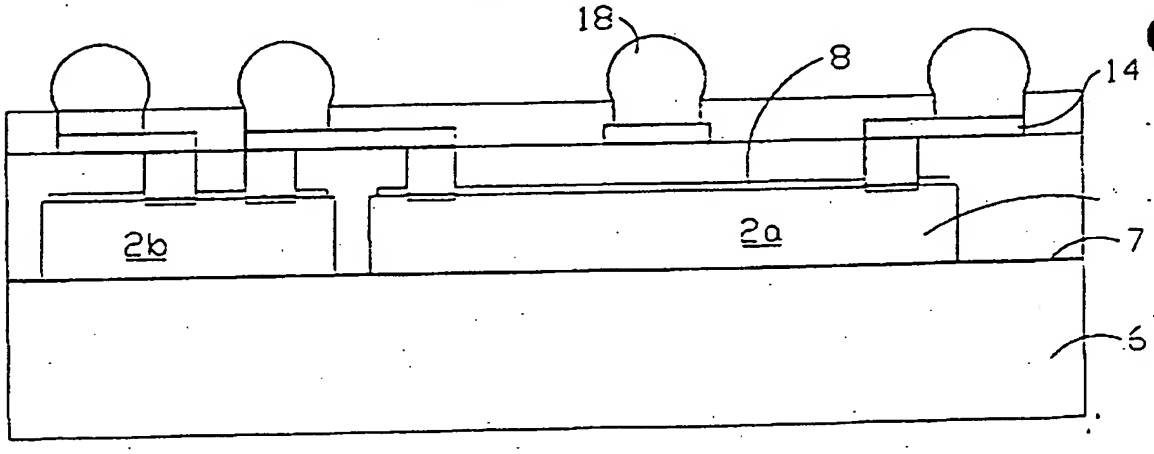


圖十七

Doc No	File (File Date)	Date	Testimony of Custodian or Qualified Witness
4	New_Technology.ppt 2002.1.15	Jan. 15th, 2002	File Author: Wen-kun Yang

Advanced Chip Engineering Technology Inc

新技術發表

裕沛科技股份有限公司

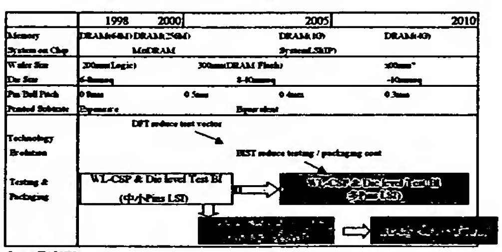
January 16th, 2002

KGD/CSP技術藍圖

此資料取自於 EIAJ 在1999年8月份發行的 Japan Jisso Technology Roadmap 1999，P235 & P233

KGD/CSP技術藍圖

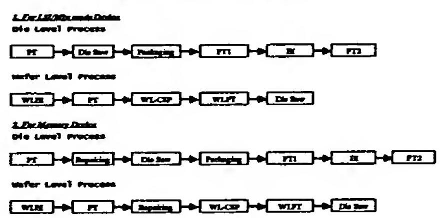
Table: KGD / CSP Technology Roadmap



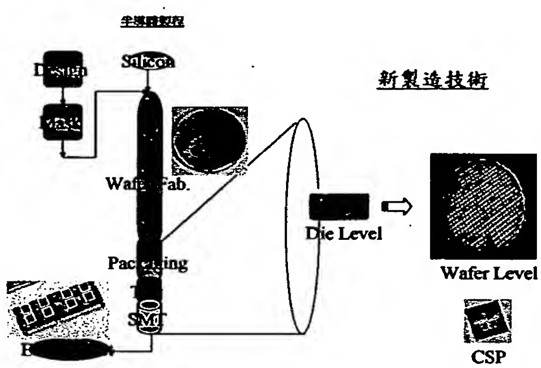
Source: EIAJ 1999

製造技術藍圖

Table: IC Back-end Process Flow Roadmap



Source: EIAJ 1999



Advanced Chip Engineering Technology Inc.
Development status

- The first WL-CSP (daisy chain)announce in Feb. 2001
- The first 64M SD WL-CSP announce in May. 2001
- The first 128Mbyte DIMM announce in August 2001
- The first WLPC for WLFT announce in Sept. 2001
- Completed the WLP production set-up in Nov. 2001
- The first 128M SD WL-CSP announce in Dec. 2001
- The first 256M byte SO-DIMM announce in Dec. 2001
- The first 256M DDR WL-CSP announce in Dec. 2001
- The first 512Mbyte DDR DIMM available on 1/16

New Technologies: **Wafer Level Technologies**

1 Wafer Level Burn In
Suitable for memory product

2 Wafer Level Packaging (ACECSP, ACEBGA)

3 Wafer Level Testing
Wafer Level Probe Card (WLPC)
For wafer sort,
wafer level final speed test,
wafer sort after bumping.

4 Wafer Level Board Assembly Process

Wafer Level Burn-in

ACE Technology Inc.

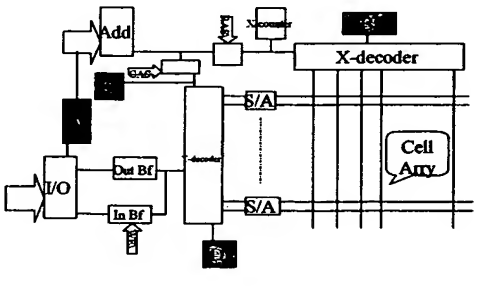
Wafer Level Burn-in

- Evolution Technology
- Good for DRAM, SRAM, Embedded Memory, Flash memory
- Need the build in circuit (design in)
- Dedicated burn-in system(64 DUTs)
- Burn-in the chip in wafer form
- Real time feedback the result to wafer process

WLBI Technology

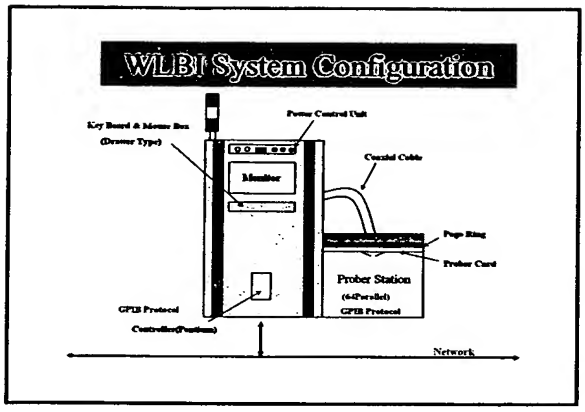
- Using the existing methodology – high voltage, high temperature, dynamic cycle.
- Detect the Infant Mortality defect at early stage.
- Design the burn-in mode to turn on-
  - Whole word lines simultaneously
  - Whole bit lines simultaneously
  - Stress the peripheral circuit
- Dedicated burn-in test system

Wafer Level Burn-In BIST Block Diagram (DRAM)



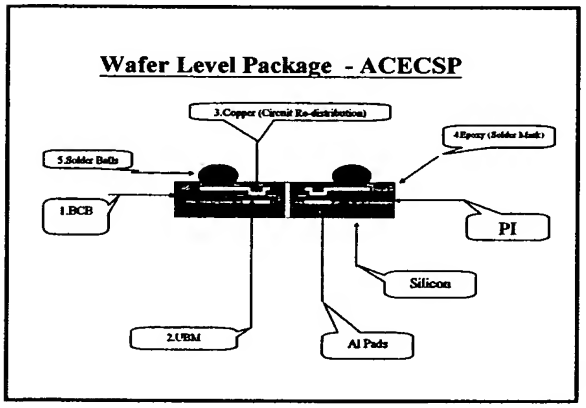
Wafer Level Burn-In vs. Traditional Burn-In

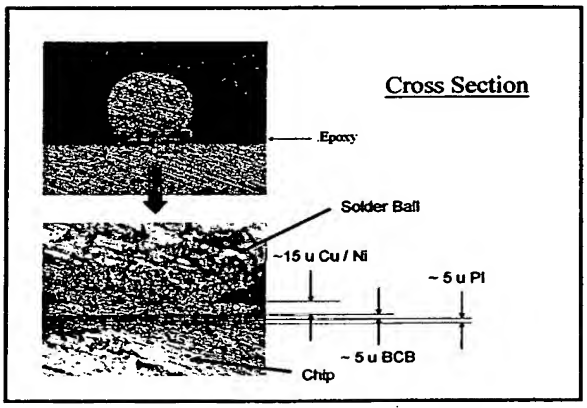
Items	WLBI	TBI
✓ *Burn-in Duration*	< 1 minutes	24 hours
✓ *Loader/Off-loader*	No Need	4 - 8 Hours
✓ *BI voltage*	Adjustable	Fix
✓ *Lot trace-ability*	Simple & Real time	Complicated
✓ *BI system*	Simple & low cost	Complicated & high cost
✓ *Qty/ Batch*	32 or 64 DUTs/time	5k - 12kpcs / oven
✓ *Tooling*	Probe card, low cost	Socket & BIBs & C/Ks
✓ *BI Circuit(Chip)*	Need built in circuit	No need
✓ *Automation*	Simple & low cost	Complicated & high cost

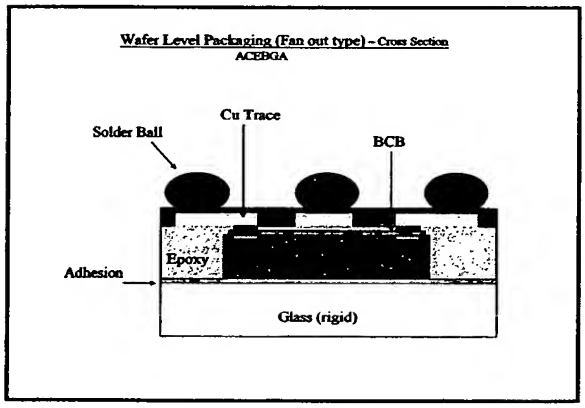


Wafer Level Packaging

ACE Technology Inc.



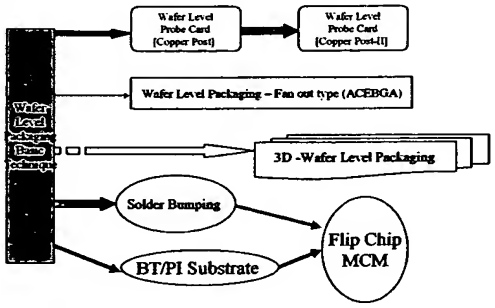


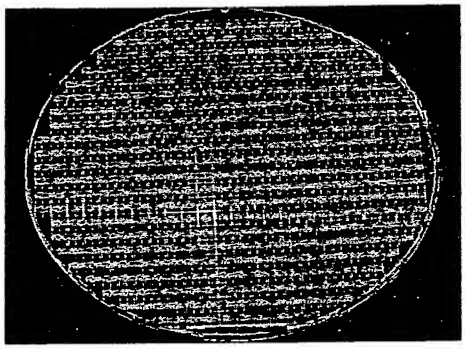


The advantage of ACE WLP

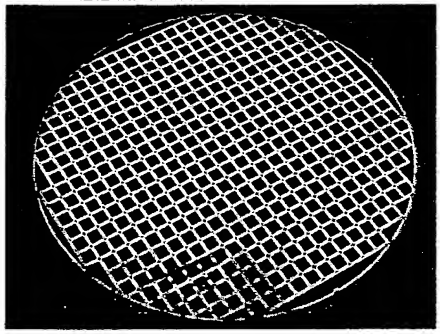
- Real Chip Size Package –No under-fill
- (same ball pitch – ACEBGA)
- Can do Wafer Level Final Testing
- The lowest cost – simple tooling & material
- Die shrink – Change mask

Wafer Level Packaging Roadmap

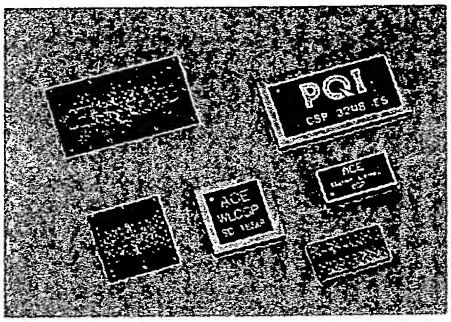




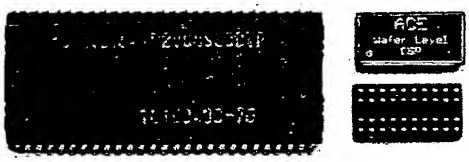
WL-CSP circuit side (solder balls array)



WL-CSP Back side (Top mark)



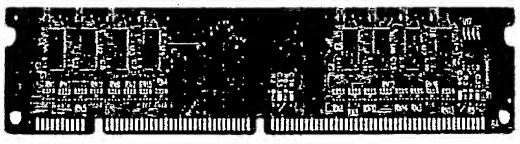
WLP Real Chip Size Package

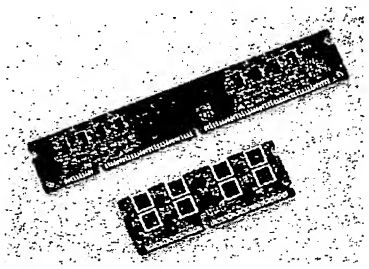


TSOP vs. WL-CSP

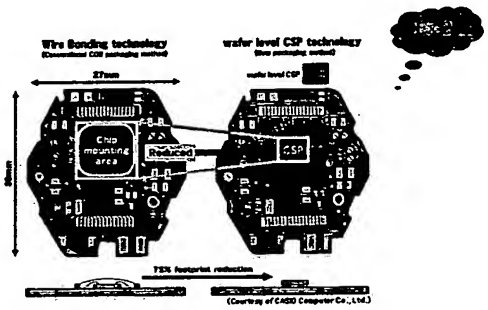
Memory Module

Using CSP Package





DIMM & SO-DIMM using CSP type



WL-CSP application – Watch (資料來源IEP)

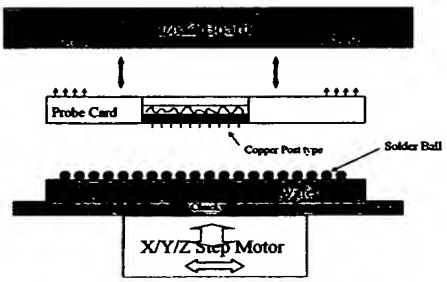
The Wafer Level Difference…

Traditional IC Packaging		*Wafer Level Packaging*
✓ Wafer probed, diced, and sorted	◄ ►	Wafer moved directly to packaging
✓ ICs packages away from fab	◄ ►	ICs packaged in fab
✓ ICs are packaged one at a time	◄ ►	ICs are packaged all at once (by wafer & lot)
✓ Burn In performed in sockets	◄ ►	Burn In performed on wafer(WLBI)
✓ Power and ground taken from PCB	◄ ►	Power and ground distributed in "Package"
✓ Device tested 2 - 3 times	◄ ►	Device tested once (Wafer level final test)
✓ High pin counts required	◄ ►	Lower external I/O possible
✓ High power required	◄ ►	Reduced power requirements
✓ All function in the chip	◄ ►	Function shared between package and chip
✓ More complex substrate required	◄ ►	No substrate possible (lower I/O)
✓ Lead inductance concerns	◄ ►	Lead inductance nearly eliminated
✓ Longer cycle time	◄ ►	Shorter cycle time (1.5 Days)
✓ Higher cost	◄ ►	Lower cost

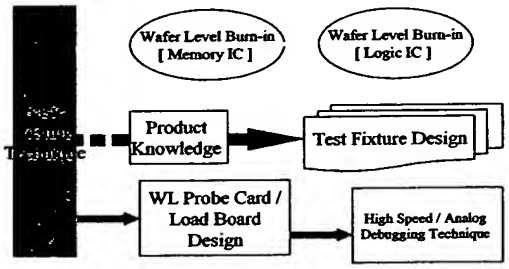
Wafer Level Testing

ACE Technology Inc.

Wafer Level Final Testing

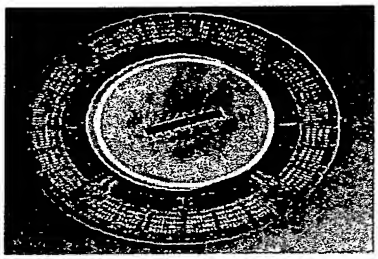


Wafer Level Testing Roadmap

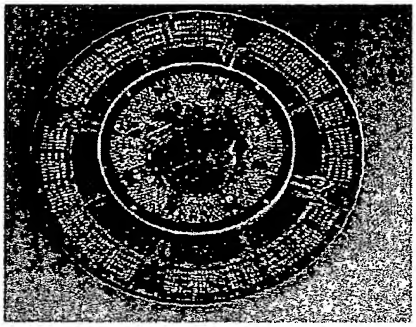


Wafer Level Probe Card

- Vertical type probe card
- Making by Chemical Process
- Can probe Al bonding pads
- Can probe Solder Balls (WL-CSP)
- Using current probing set-up
- Can build up high pin count probing
- Suitable for high speed, high power probing



WLPC 2x8 devices (128MSD) for T5335P

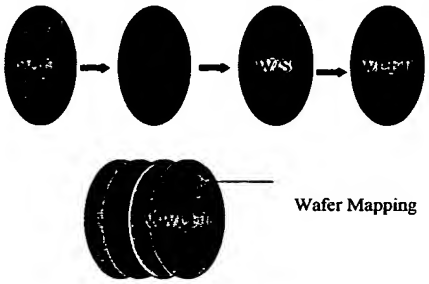


WLPC (pogo pins type) 8 devices for T5382A

The Advantage by using wafer level

- Reduce the Cycle time in Back-end
  - From 14-20 days to 5-7 days
- Simple Tooling – Probe Card & Masks
- Prevent the process errors in advance
- Reduce the Back-end cost
  - Reduce the tooling & machine & socket
  - Reduce the machine index time
  - Reduce the materials

Prevent the Process errors in advance



KGD/CSP Solution

- Using Wafer level process technology
  - Wafer level probe card solution
- Speed sorting at wafer level
- Performance evaluation at wafer level
- Perform wafer level burn-in for die sale -Quality
- Die sorting by using wafer mapping
- Can test wafer after bumping
- Easy handling during process – wafer form

裕沛科技以自行研發的新製造技術提供半導體產業在後段製程(封裝、測試、組裝－輕、薄、短、小、高速、高整合)與微機電產品等 完整的技術與服務。
ACE is your long term Partner。

Thanks

Affidavit of Facts

I, Wen-kun Yang (楊文焜), am a C.E.O of ACE (Advanced Chip Engineering Technology Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No. 65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu 303, Taiwan, R.O.C.

I hereby attest that, on January 15, 2002. I have completed the file "New_Technology.ppt", it has been used as presentation file during the open house of ACET on Jan. 16th, 2002 once Advanced Chip Engineering Technology Inc. has moved to his own building in Industrial Park and to announce the new technology during the open house. At that time, I chair the open house and also present the file.

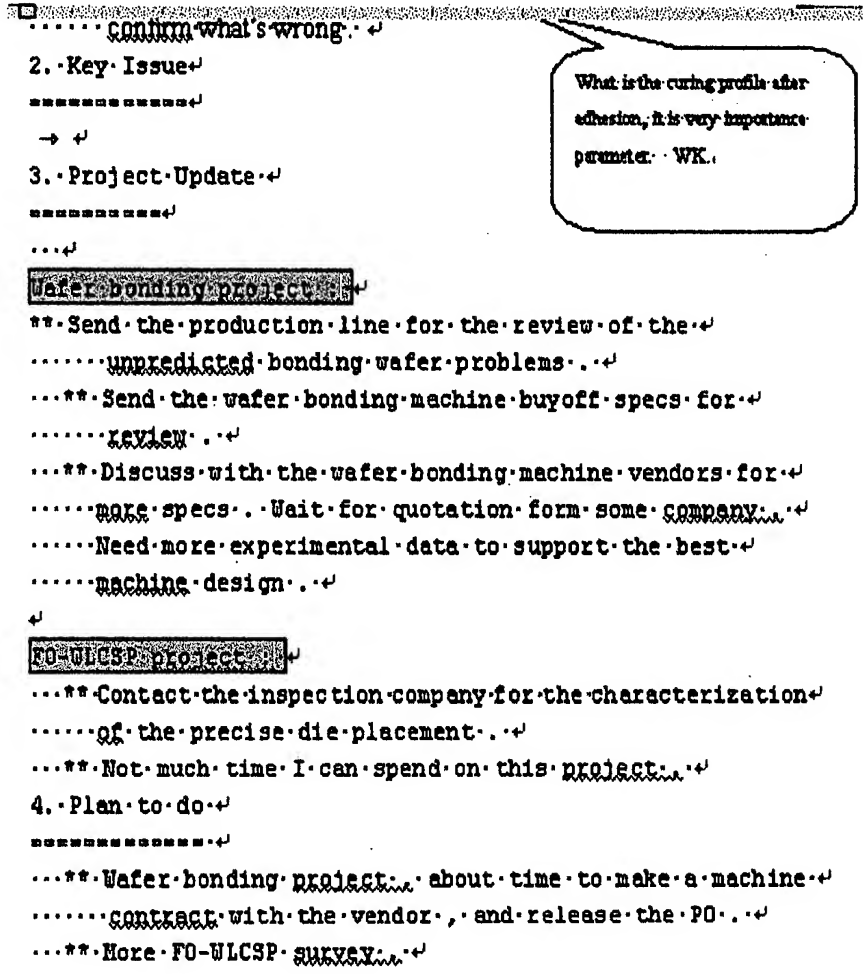
I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature 

Date Sept. 11, 2006

Doc No	File (File Date)	Date	Testimony of Custodian or Qualified Witness
5	WEEKLY REPORT FOR 40TH WEEK.DOC 2002.10.8	Oct. 8th, 2002	Reporter: Roger Chiu
	ROGER_REPORT_1.DOC 2002.12.16	Dec. 16th, 2002	Reporter: Roger Chiu

FO-WLP – Project development starting Date



Working week 40 /2002
RD report
On Oct. 8th, 2002

Weekly report for 40th week Oct. 8th, 2002

1. Highlight :

==========

** We found the Si (300 um) + glass (200 um) has good adhesion but big warpage , about 500 um of warpage . We think that the warpage is coming from glass , the glass CTE from the glass vendor is about 4.5x10 (-6) , by calculation , this CTE won't cause warpage of more than 50 um for 8 inch wafer , (Si CTE ~ 3x10 (-6)) , something is wrong with the real CTE , need time to confirm what's wrong .

What is the curing profile after adhesion, it is very importance parameter. WK

2. Key Issue

==========

3. Project Update

==========

Wafer bonding project :

** Send the production line for the review of the unpredicted bonding wafer problems .

** Send the wafer bonding machine buyoff specs for review .

** Discuss with the wafer bonding machine vendors for more specs . Wait for quotation form some company . Need more experimental data to support the best machine design .

FO-WLCSP project :

** Contact the inspection company for the characterization of the precise die placement .

** Not much time I can spend on this project .

4. Plan to do

==========

** Wafer bonding project , about time to make a machine contract with the vendor , and release the PO .

** More FO-WLCSP survey .

Dec. 16th, 2002

Roger_Report_1

We have talked about using real wafer (4 Mb DRAM or something) as the test vehicle for the precise die placement verification , please let me know how could I get the test vehicle ???

I am planning to send them to the machine vendor for prototyping .

Amkor Expanding VisionPak Image Sensor Packaging for a Growing Market

CHANDLER, Ariz. -- Nov. 5, 2002--Amkor Technology (Nasdaq: AMKR) is expanding its VisionPak(TM) CMOS image sensor assembly capabilities in order to meet increasing demand for high quality, video and digital camera features in digital and PC cameras, cell phones and other hand-held applications.

Industry analyst In-Stat estimates the market for CMOS image sensors will increase rapidly from 19 million units in 2001 to 35 million units in 2002 and more than 140 million units in 2005. The most significant growth should occur through the integration of image sensors into cell phones, where In-Stat estimates the market will explode from 3.8 million units in 2001 to 10 million units in 2002 and more than 62 million units in 2005. Amkor estimates that approximately 60% of CMOS image sensor packaging is presently outsourced.

Amkor has been expanding its vision sensor capabilities through a state-of-the-art assembly facility in Taiwan that is now in high volume operation. For 2002, Amkor expects to produce more than 4 million VisionPak CMOS image sensor packages, representing approximately 13% of the total CMOS image sensor market and 22% of the outsourced market, making Amkor the largest outsourced supplier of CMOS image sensor packaging outside of Japan.

Amkor offers the growing CMOS image sensor market two types of vision package technologies. The first is a traditional image sensor package called a ceramic leadless chip carrier, or CLCC. This cavity style package is generally a single chip solution, but can be adapted for multi chip. Amkor established its VisionPak CLCC product line in late 1999 through close collaboration with a major U.S.-based supplier of CMOS image sensor devices.

With the knowledge gained in the early development of its CLCC sensor packages, Amkor expanded the scope of its image packaging solutions to provide a second, more advanced type of vision package: the fully integrated camera module. The VisionPak camera module

typically consists of multiple components including CMOS image sensor die, passives, infrared filter glass, lens mount, and lens barrel, and sometimes a separate driver IC.

Amkor expects to produce more than 300 thousand VisionPak camera modules in 2002 and recently expanded its VisionPak camera module assembly facility in Taiwan.

Amkor's proprietary module assembly process implants lens assemblies onto the module housing and substrate. Then Amkor uses focus-and-lock testing technology to create a fully integrated image sensor assembly and focus line that optimizes the production flow and reduces cycle time. Amkor's integrated process leverages the company's existing infrastructure for wire bond and surface mount assembly.

Camera modules are typically customized to the customer's end-product application. CMOS image sensor modules are available in CIF, VGA, and in the future, MEGA pixel formats, depending on the design of the silicon die inserted into the package. The modules typically use the higher density VGA format, which capture video and/or photographs. By using the higher density image sensor die in its VisionPak, Amkor is able to increase the image quality without increasing the dimensions of the package.

"Camera modules have traditionally been produced internally by the large Japanese electronics companies. We've been working hard to develop innovations that will help reduce the packaging and focus costs for camera modules, which in turn should promote more outsourcing," said Mike Steidl, vice president of Amkor's advanced product development. "We believe our image sensor assembly and test capabilities should position Amkor to capture an attractive share of the rapidly growing market for portable imaging applications."

For a 2x 2 mm die size image sensor chip , the current package size is PLCC 9x9 mm,
each package market price is about 20 NTD . That means , each 8 inch image sensor wafer has
a package price of about 3600 USD (You can't imagine this is true , and the
package price is even higher than the wafer price) .
If we fan out 2x2 mmto 5x5 mm FO-WLCSP , we need 6.25 FO-WLCSP ,
that means , each FO-WLCSP can have a price of 576 USD ,
this will be much attarctive and profit-gaining market
than the mini BGA .
So , if you are talking about FO-WLCSP , this is more likely the
value-added market .

育霈科技股份有限公司
Advanced Chip Engineering Technology Inc.

離職證明書
Resignation Certification

姓　名 Name	邱肇廷 Roger Chiu	出生日期 Date of Birth	民國50年03月11日 11-Mar-61
身份證字號 I.D. No	H120099421	性　別 Sex	男 Male
服務部門 Department	研發一處 R&D I Div.	職　稱 Job Title	工程師 Engineer
到職日 Date of Employment	民國91年04月08日 08-Apr-02	離職日 Date of Leaving	民國92年02月06日 06-Feb-03
備　註 Remark	空白 Nil		

上述各項屬實，特此證明。
This is to certify that the above statements are true and correct.

人力資源部
Human Resources Department

育霈科技股份有限公司 人事專用章 新竹縣湖口鄉光復北路65號

中華民國九十五年八月十四日
Date：August 14, 2006

地址：新竹縣303新竹工業區光復北路六十五號　電話:03-5983232
Add： No.26, Kuang-Fu North Rd., Hsin-Chu Industrial Park, Hsin-Chu 303, Taiwan, R.O.C.
TEL：886-03-5983232　FAX：886-5986565

Doc No	File (File Date)	Date	Testimony of Custodian or Qualified Witness
6-1	714_2003.doc	Jul. 14th, 2003	Conferee: Wen-kun Yang, DC Huang, Co Co Kow, Kathy Lin, Ben Lin, Eva Chiou, Alex Chen,Yatzu Wu Chairman: Bob Chen Conference Recorder: Bob Chen Copy Receiver: David Lin, Jalex Sun, MJ Chiu
6-2	Weekly Report 030.doc	Jul. 21st ~Jul. 25th, 2003	File Author: Bob Chen
6-3	PROJECT CODE_2003.DOC 2003.7.29	Jul. 29th, 2003	Project Code Assigner: Wen-kun Yang
6-4	pscreport.ppt	Jul. 30th, 2003	File Author: Bob Chen
6-5	20030801.doc 2006.6.26	Aug. 1st, 2003	Chairman: Wen-kun Yang Recorder: Bob Chen Participants: David、Eva、Yatzu、Ben、Alex Chen、Jalex、Alex Long Copy Receiver: Eddy Mo、Yao Hung、David Lin、Liching Huang
6-6	MEETING MINUTES OF 300MM W.DOC 2003.8.8	Aug. 8th, 2003	Participants: WK, Yao, Ben, Jalex
6-7	300MM WAFER HANDLING CASE.DOC 2003.9.22	Sep. 22nd, 2003	File Author: Wen-kun Yang
6-8	300MM WAFER FOR WL-CSP PRO.XLS 2003.9.29	Sep. 29th, 2003	

6 - 1

FO-WLP – Project development Meeting contents

會議內容	
1. 計畫目的	
2. 目前進度說明 (. 可行性評估)	
3. 預計量產進度說明 (. Q4量產)	
4. 研發資源需求 (. 人力及設備)	
5. 各部門配合事項說明 (. 12"wafer, 玻璃基板及矽膠備料)	
6. 討論及協調事項	
7. 決議及結論	
決議及結論	
1. 玻璃基板及矽膠光阻等新材料備料	寇宗森, 孫文彬
2. 量產製程開發	林源斌, 吳雅慈, 林明耀, 孫文彬
3. 信賴度樣品及測試	周玲如, 林明耀
4. 工程及研發人力調配協調	吳雅慈, 林源斌, 陳世立
5. 製程人員補充及培訓	黃德權, 林源斌
6. PSC聯絡窗口	林誼芳
7. 研發計畫進度控管	陳世立

July 14th, 2003
Chair by: Bob

裕沛科技股份有限公司

內部會議記錄

2003

會議名稱	12" to 8" 計畫協調說明會	時間	7月14日下午2時
		地點	503
召集單位及主席	陳世立	記錄	陳世立
重要出席人員	楊文焜,黃德權,寇宗森,林誼芳,林源斌,周玲如,陳昊天,吳雅慈,陳世立		
副本分送	林明輝,孫文彬,邱梅珍		
附件			

決議事項	承辦人員	應結日期

File: 714.doc

裕沛科技股份有限公司

內部會議記錄

會議內容		
1. 計畫目的 2. 目前進度說明 (可行性評估) 3. 預計量產進度說明 (Q4量產) 4. 研發資源需求 (人力及設備) 5. 各部門配合事項說明 (12"wafer, 玻璃基板及矽膠備料) 6. 討論及協調事項 7. 決議及結論		
決議及結論		
1. 玻璃基板及矽膠光阻等新材料備料	寇宗森, 孫文彬	
2. 量產製程開發	林源斌,吳雅慈, 林明輝,孫文彬	
3. 信賴度樣品及測試	周玲如,林明輝	
4. 工程及研發人力調配協調	吳雅慈, 林源斌, 陳世立	
5. 製程人員補充及培訓	黃德權,林源斌	
6. PSC聯絡窗口	林誼芳	
7. 研發計畫進度控管	陳世立	
附註:濺鍍站因設備自動進料零件尚未收到,邱梅珍預計八月後再調回RD1,目前排列晶片工作以加班方式進行。		

批示	

附註: 紅字日期為延遲完成之日期

Affidavit of Facts

I, Bob Chen (陳世立) , was a RD Center Leader of ACE (Advanced Chip Engineering Inc.)formerly, a company organized under the laws of Taiwan, R.O.C., and having a business address of No.65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu, Taiwan, R.O.C.

In 2003, Mr. Yang assigned me to be the project leader of new technology development –FO-WLP. At 2:00pm, on July 14, 2003, I hosted the meeting for Fan-out wafer level packaging (i.e. 2G Technology). I made the statement about project process executing and manpower arrangement in the meeting minutes. I hereby attest that the content of minutes I wrote is true.

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature Bob Chen

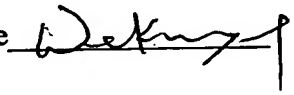
Date Sep. 11. 2006

Affidavit of Facts

I, Wen-kun Yang (楊文焜), am a C.E.O of ACE (Advanced Chip Engineering Technology Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No. 65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu 303, Taiwan, R.O.C.

I hereby attest that, on July 14, 2003. I have attended the meeting that chaired by Mr. Bob Chen who is the project leader of Fan-out wafer level packaging, during the meeting Bob has assigned the team members and his responsibility. At that time, I am the CEO/Chairman of this company and assign Mr. Bob Chen as project leader of new technology development – FO-WLP。

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature 

Date Sept. 11, 2006

Affidavit of Facts

I, Kathy Lin(林誼芳) , am a Project Manger of ACE (Advanced Chip Engineering Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No.65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu, Taiwan, R.O.C.

I hereby attest that, on July 14, I attended the meeting for 12" transfer 8" FO-WLP Project. In that project, my duty was the window of wafer supplier.

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature Kathy Lin

Date Sept. 14. 2006.

Affidavit of Facts

I, Ben Lin(林源斌) , am a Assistant Manger of ACE (Advanced Chip Engineering Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No.65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu, Taiwan, R.O.C.

I hereby attest that, in Year 2003, I was responsible for engineering and manpower coordination in 12" transfer to 8" FO-WLP Project. And on July 14, 2003, I attended the project review meeting that Bob chaired.

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature 林源斌 Ben Lin

Date 9/13/06

Affidavit of Facts

I, Jalex Sun (孫文彬) , am a Technical Manger of ACE (Advanced Chip Engineering Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No.65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu, Taiwan, R.O.C.

I hereby attest that, July 14, 2003, I didn't attend the meeting for 12" transfer 8" FO-WLP Project. After meeting, I got the minutes for the meeting conclusion.

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature 孫文彬 Jalex Sun

Date 9/13.

Affidavit of Facts

I, Yatzu Wu (吳雅慈) , am a Product Manger of ACE (Advanced Chip Engineering Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No.65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu, Taiwan, R.O.C.

I hereby attest that, on July 14, 2003, I took part in the meeting of 12" transfer to 8" wafer FO-WLCSP. I was in charge of lithography part in process development.

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature 吳雅慈 Yatzu Wu

Date 2006/09/15

Affidavit of Facts

I, MJ Chiu (邱梅珍) , am a Senior Technician of ACE (Advanced Chip Engineering Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No.65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu, Taiwan, R.O.C.

I hereby attest that, July 14, 2003, I didn't attend the meeting for 12" transfer 8" FO-WLP Project.. After meeting, I received the minutes.

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature 邱梅珍 MJ. Chiu

Date 9/5 06

育霈科技股份有限公司
Advanced Chip Engineering Technology Inc.

離職證明書
Resignation Certification

姓　名 Name	黃德權 DC Huang	出生日期 Date of Birth	民國50年07月26日 26-Jul-61
身份證字號 I.D. No	J122648503	性　別 Sex	男 Male
服務部門 Department	行政支援處 Administration Supporting Div.	職　稱 Job Title	資深處長 Senior Director
到職日 Date of Employment	民國90年10月15日 15-Qct-01	離職日 Date of Leaving	民國94年05月10日 10-May-05
備　註 Remark	空白 Nil		

上述各項屬實，特此證明。
This is to certify that the above statements are true and correct.

人力資源部
Human Resources Department

育霈科技股份有限公司 人事專用章 新竹縣湖口鄉光復北路65號

中華民國九十五年八月十四日
Date：August 14, 2006

地址：新竹縣303新竹工業區光復北路六十五號　電話:03-5983232
Add： No.26, Kuang-Fu North Rd., Hsin-Chu Industrial Park, Hsin-Chu 303, Taiwan, R.O.C.
TEL：886-03-5983232　FAX：886-5986565

育霈科技股份有限公司
Advanced Chip Engineering Technology Inc.

離職證明書
Resignation Certification

姓　名 Name	寇宗森 Co Co Kow	出生日期 Date of Birth	民國51年2月11日 11-Feb-62
身份證字號 I.D. No	J220158786	性　別 Sex	女 Female
服務部門 Department	採購/進出口部 Purchasing/Import& Export Dept.	職　稱 Job Title	經理 Manager
到職日 Date of Employment	民國89年5月15日 15-MAY-00	離職日 Date of Leaving	民國95年3月10日 10-Mar-06
備　註 Remark	空白 Nil		

述各項屬實，特此證明。
This is to certify that the above statements are true and correct.

人力資源部
Human Resources Department

育霈科技股份有限公司 人事專用章 竹縣湖口鄉光復北路65號

中華民國九十五年八月十一日
Date：August 11, 2006

地址：新竹縣303新竹工業區光復北路六十五號　電話:03-5983232
Add： No.26, Kuang-Fu North Rd., Hsin-Chu Industrial Park, Hsin-Chu 303, Taiwan, R.O.C.
TEL：886-03-5983232　FAX：886-5986565

育霈科技股份有限公司
Advanced Chip Engineering Technology Inc.

離職證明書
Resignation Certification

姓　名 Name	周玲如 Eva Chou	出生日期 Date of Birth	民國59年01月22日 22-Jan-70
身份證字號 I.D. No	J220173854	性　別 Sex	女 Female
服務部門 Department	先進技術研發處 Advanced Technology Div.	職　稱 Job Title	技術經理 Technical Manager
到職日 Date of Employment	民國89年04月17日 17-Apr-00	離職日 Date of Leaving	民國95年07月28日 28-Jul-06
備　註 Remark	空白 Nil		

上述各項屬實，特此證明。
This is to certify that the above statements are true and correct.

人力資源部
Human Resources Department

育霈科技股份有限公司 人事專用章 新竹縣湖口鄉光復北路65號

中華民國九十五年八月十四日
Date：August 14, 2006

地址：新竹縣303新竹工業區光復北路六十五號　電話:03-5983232
Add： No.26, Kuang-Fu North Rd., Hsin-Chu Industrial Park, Hsin-Chu 303, Taiwan, R.O.C.
TEL：886-03-5983232　FAX：886-5986565

育霈科技股份有限公司
Advanced Chip Engineering Technology Inc.

離職證明書
Resignation Certification

姓　名 Name	陳昊天 Alex Chen	出生日期 Date of Birth	民國61年07月28日 28-Jul-72
身份證字號 I.D. No	G120620845	性　別 Sex	男 Male
服務部門 Department	測試工程部 Testing Engineering Dept.	職　稱 Job Title	經理 Manager
到職日 Date of Employment	民國89年04月21日 21-Apr-00	離職日 Date of Leaving	民國94年05月06日 06-May-05
備　註 Remark	空白 Nil		

上述各項屬實，特此證明。
This is to certify that the above statements are true and correct.

人力資源部
Human Resources Department

育霈科技股份有限公司 人事專用章 新竹縣湖口鄉光復北路65號

中華民國九十五年八月十四日
Date：August 14, 2006

地址：新竹縣 303 新竹工業區光復北路六十五號　電話:03-5983232
Add： No.26, Kuang-Fu North Rd., Hsin-Chu Industrial Park, Hsin-Chu 303, Taiwan, R.O.C.
TEL：886-03-5983232　FAX：886-5986565

育霈科技股份有限公司
Advanced Chip Engineering Technology Inc.

離職證明書
Resignation Certification

姓　名 Name	林明輝 David Lin	出生日期 Date of Birth	民國62年03月17日 30-Aug-76
身份證字號 I.D. No	K120404657	性　別 Sex	男 Male
服務部門 Department	製程工程處 Process Engineering Div.	職　稱 Job Title	技術副理 Technical Assistant Manager
到職日 Date of Employment	民國90年02月26日 26-Feb-01	離職日 Date of Leaving	民國94年11月30日 30-Nov-05
備　註 Remark	空白 Nil		

述各項屬實，特此證明。
This is to certify that the above statements are true and correct.

人力資源部
Human Resources Department

育霈科技股份有限公司 人事專用章 新竹縣湖口鄉光復北路65號

中華民國九十五年八月十一日
Date：August 11, 2006

地址：新竹縣303新竹工業區光復北路六十五號　電話:03-5983232
Add： No.26, Kuang-Fu North Rd., Hsin-Chu Industrial Park, Hsin-Chu 303, Taiwan, R.O.C.
TEL：886-03-5983232　FAX：886-5986565

6 - 2

週次：30　　裕沛科技股份有限公司　　應出勤日數： 5 日

2003　90年7月21日～7月25日　　工作週報表　　實際出勤日數： 5 日

目標項目或工作項目(名稱)	本期執行狀況(含進度說明、差異分析)	負責人	下期預定工作重點及其他說明
1. WLCSP BIB	● 與KYEC安排檢驗高溫 burn-in 情況：高溫區矽油洩漏，無法加壓，需重新製作彈簧夾具。	RD1 / RD2	● 彈簧夾具製作。 ● 與KYEC安排高溫 burn-in 時間。 ● 檢驗高溫 burn-in 情況。 ● PCB 重新 layout / 發包 / 製作。 ● WL-CSP burn-in 測試 / 驗收。
2. 12' to 8' Wafer FO-WLCSP	● 第一片進行至SM顯影。 ● 完成（第二片）SINR長方形開孔設計，顯影情況、良率及精確度良好。	RD1	● 玻璃基板延期交貨(7/31)。 ● 調整晶片間隙填充矽膠網板設計，消除氣泡包覆影響。 ● 修改光罩及治具對位記號。 ● Wafer 切割評估。 ● 完成 ink die WLCSP 製程評估。 ● 製作玻璃光罩。 ● 採購 PSC 12" 0.13 u 256 M DDR good die。 ● 進行 good die WLCSP 製程良率評估。 ● 進行 pkg.及 on board 信賴度評估。
3. 8' Wafer with Glass Substrate	● 收到兩種 UV 矽膠樣品及 300u wafer。 ● 完成三種網板印刷圖案設計並發包。		● 印刷三種 UV 矽膠圖案，並進行貼合玻璃基板測試。 ● 進行 BCB / sputter / plating / solder ball mount 等標準製程參數測試。 ● Wafer 切割評估。 ● 設計玻璃基板貼合治。 ● 進行 good die WLCSP 製程良率評估。 ● 進行 pkg.及 on board 信賴度評估。

主管：　　填表人：Bob

File：Weekly Report030.doc

Affidavit of Facts

I, Bob Chen (陳世立) , was a RD Center Leader of ACE (Advanced Chip Engineering Inc.) formerly, a company organized under the laws of Taiwan, R.O.C., and having a business address of No.65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu, Taiwan, R.O.C.

I hereby attest that, on July 21 to 25, 2003, I was in charge of three projects that I mentioned in the weekly report. They are *a.* WLCSP BIB *b.* 12" to 8" wafer FO-WLP *c.* 8" wafer with glass substrate.

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature Bob Chen

Date Sep. 11. 2006

6 - 3

July 29th, 2003

Project Code_2003

	Project leader	Project Code
1. WL-CSP BIB	Bob	9211
2. 300mm wafer for WL-CSP	Bob	9222
3. Pogo probe card for Agilent test system	David	9233
4. PC based tester for WL-CSP final testing	David	9234
5. 200mm Glass based WL-CSP	Bob	9235

Affidavit of Facts

I, Wen-kun Yang (楊文焜), am a C.E.O of ACE (Advanced Chip Engineering Technology Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No. 65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu 303, Taiwan, R.O.C.

I hereby attest that, on July 29, 2003, I have assigned the project code numbers for the projects of the company, at that time, I am the CEO of the company and have started the several projects for new development which including the FO-WLP。。

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature 

Date Sept. 11, 2006

6 - 4

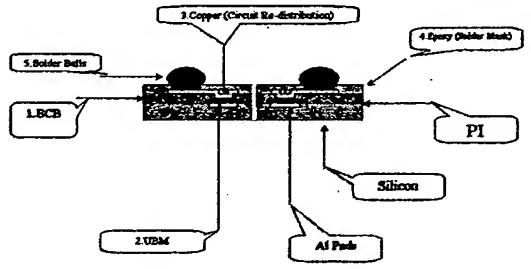
July. 30th, 2003
File: pscreport.ppt

FO-WLCSP
(12" to 8" Wafer)

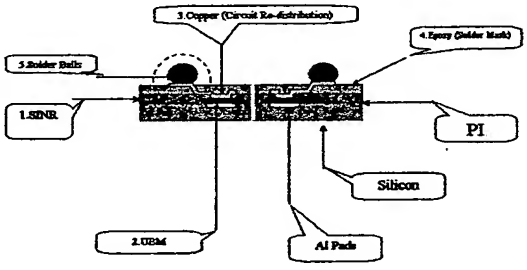
ACET WLCSP Technology Roadmap

	2000	2002 / 2003	2003 / 2004	2004 / 2005	2005/2010
Memory	64M SDRAM	256M SDRAM	256M DDR SDRAM	512M DDRII SDRAM	> 1G
Gate Size	0.18 u	0.18 u / 0.15	0.13 u / 0.11	0.11 u / 0.09 u	< 0.06 u
Max. speed	133 MHz	166 MHz	400 / 600 MHz	800/ 850 MHz	> GHz
WL-CSP	G1-WLCSP		FO-WLCSP	G2-WLCSP	MC-WLCSP

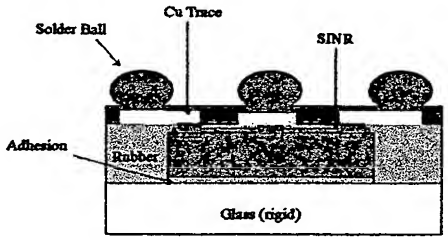
G1 WLCSP



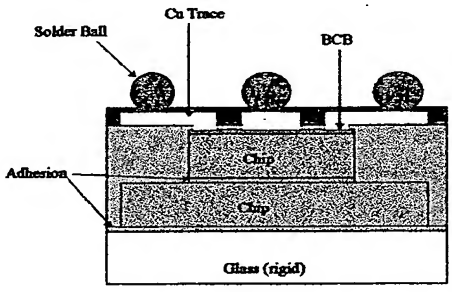
G2 WLCSP



FO WLCSP

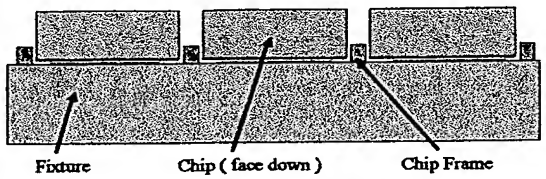


MC WLCSP

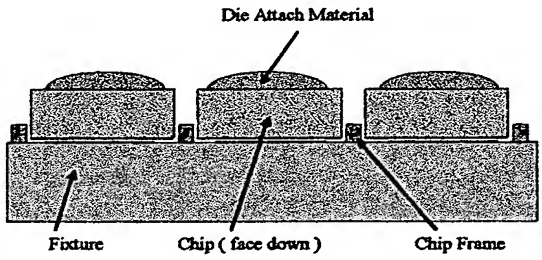


FO-WLCSP
Process

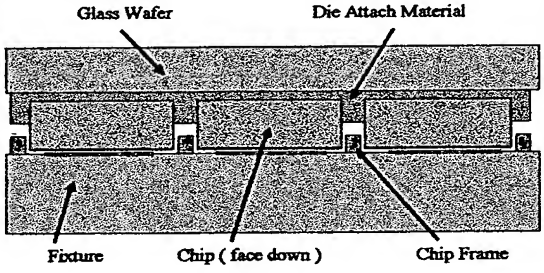
ALIGN CHIP ON FIXTURE



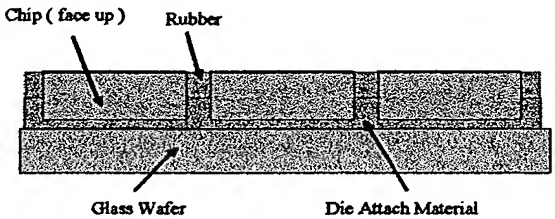
DISPENSE DA MATERIAL ON CHIP BACK SIDE



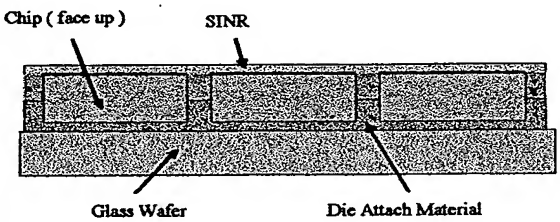
ATTACH GLASS WAFER TO ALIGNED CHIPS

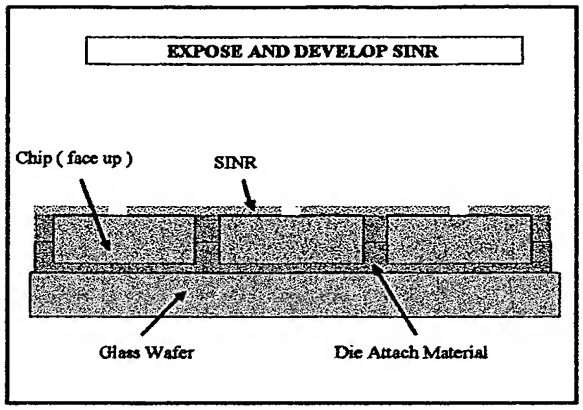


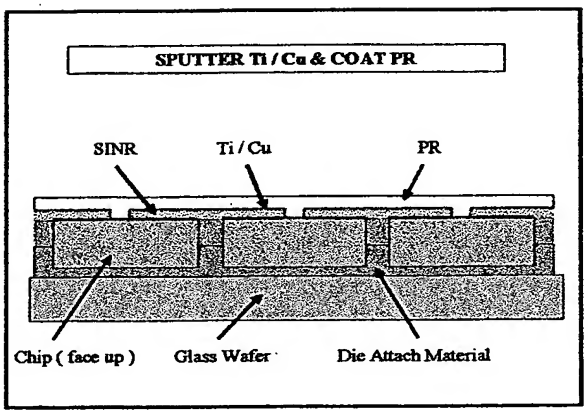
PRINT RUBBER

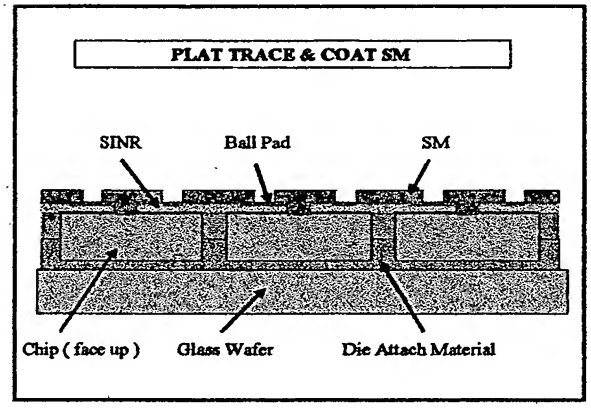


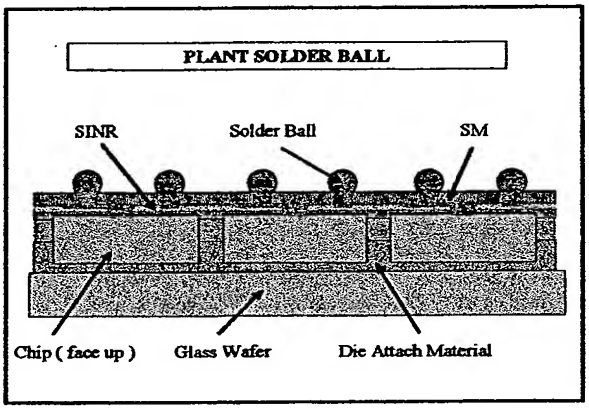
COATING SINR

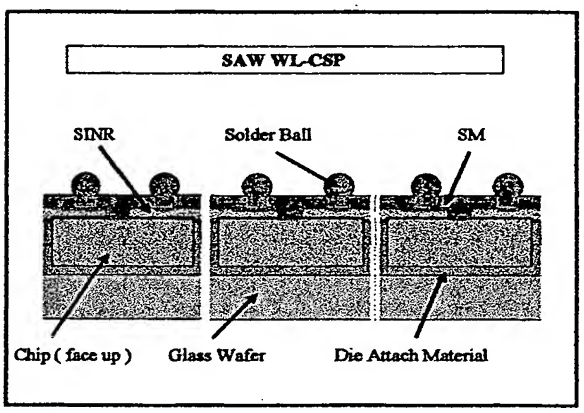


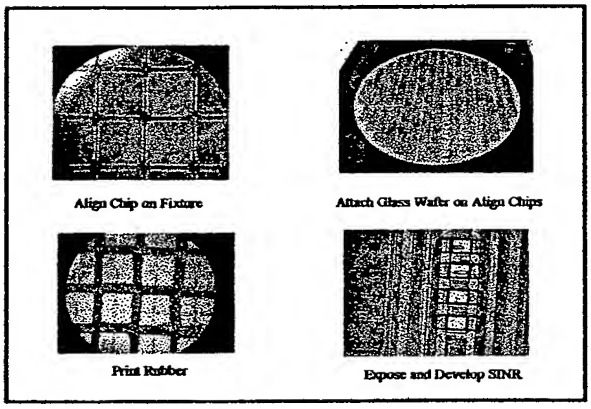

EXPOSE AND DEVELOP SINR
Chip (face up)
SINR
Glass Wafer
Die Attach Material


SPUTTER Ti / Cu & COAT PR
SINR
Ti / Cu
PR
Chip (face up)
Glass Wafer
Die Attach Material


PLAT TRACE & COAT SM
SINR
Ball Pad
SM
Chip (face up)
Glass Wafer
Die Attach Material


PLANT SOLDER BALL
SINR
Solder Ball
SM
Chip (face up)
Glass Wafer
Die Attach Material


SAW WL-CSP
SINR
Solder Ball
SM
Chip (face up)
Glass Wafer
Die Attach Material


Align Chip on Fixture
Attach Glass Wafer on Align Chips
Print Rubber
Expose and Develop SINR

FO-WLCSP
Status

- Mechanical sample: 8/1
- Proto-type layout verification (on ink die): 8/8
- Reliability test: 9/E
- Process parameter fine tune(yield improve): 8/E
- Pilot Run: 9
- Mass production: 10

Affidavit of Facts

I, Bob Chen (陳世立) , was a RD Center Leader of ACE (Advanced Chip Engineering Inc.) formerly, a company organized under the laws of Taiwan, R.O.C., and having a business address of No.65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu, Taiwan, R.O.C.

I hereby attest that, on July 30, 2003, I created the presentation file of FO-WLCSP (12" to 8") including the roadmap and production schedule, etc. And I presented the procedure of FO-WLCSP to the related colleagues. It is used for the internal discussion.

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature Bob Chen

Date Sep. 11, 2006

6 - 5

裕沛科技股份有限公司

內部會議記錄 2003

會議名稱	RD Project Review	時間	7月31日上午10時 8月.1日下午2時
召集單位及主席	楊文琨	記錄	陳世立
重要出席人員	王誌榮，周玲如，吳雅慈，林源彬，陳昊天，孫文彬，龍俊均		
副本分送	牟慶聰，洪乾耀，林明輝，黃麗卿		
附件			

決議事項	承辦人員	應結日期
1. 300 mm Wafer Project		
- Glass wafer 切一大一小斜邊供定位用。	孫文彬	8/5
- 檢驗 wafer 上周邊 chip 良率，確定每片 wafer chip 數量。	林明輝，吳雅慈	
- 每一片 glass wafer 需有 ID，可在 glass 上使用 laser 編碼，再切割後與 chip 同時黏貼。		
- 測試在 glass wafer 印刷黑膠斜邊 (不透光)作爲定位用。	孫文彬，林源彬	8/5
- 300 mm wafer saw 初期由 KYEC 代工，但 pick & place 並無機台，力成有 300 mm chip sorter，可可洽詢代工可能性。		
- 直接使用 400u / 500u glass wafer，測試並定出切割道規格及 chip 切割後邊緣規格。	林源彬	
- 測試並定出 wafer saw 機台規格。	林源彬	
2. 300 u wafer project		
- 貼合烘烤三片 128M no yield 300 u wafer + 300 u dummy wafer。	孫文彬	8/5
- 量產製程驗證。	吳雅慈	

裕沛科技股份有限公司

內部會議記錄

3. BIB project - 進行 PCB layout。 - 進行高溫測試。 - 協調調回研發人員。		
批示		

附註: 紅字日期為延遲完成之日期

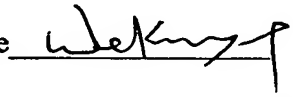
File name : 20030801.doc

Affidavit of Facts

I, Wen-kun Yang (楊文焜), am a C.E.O of ACE (Advanced Chip Engineering Technology Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No. 65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu 303, Taiwan, R.O.C.

I hereby attest that, on July 31 and August 1, 2003. I have held and chaired the "RD Project Review meeting" – the project 1 - 300mm wafer project has been used for the pre-study of FO-WLP due to the current equipments can only handle 200mm size, but the customer (DRAM maker) would like to offer the 300mm wafer size, so, the project is dicing saw the 300mm wafer and re-placement the dice on 200mm size panel and becomes the equivalent 200mm wafer size, then it can be process as wafer level packaging.

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature 

Date Sept. 11, 2006

Affidavit of Facts

I, Bob Chen (陳世立) , was a RD Center Leader of ACE (Advanced Chip Engineering Inc.) formerly, a company organized under the laws of Taiwan, R.O.C., and having a business address of No.65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu, Taiwan, R.O.C.

I hereby attest that, on July 31 and August 1, 2003, I took part in the RD Project Review Meeting that WK Yang chaired. I was in charge of the minutes at the conference and fellow up all unsettled events.

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature Bob Chen

Date Sep. 11, 2006

Affidavit of Facts

I, Ben Lin(林源斌) , am a Assistant Manger of ACE (Advanced Chip Engineering Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No.65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu, Taiwan, R.O.C.

I hereby attest that, in Year 2003, I was responsible for engineering and manpower coordination in 12" transfer to 8" FO-WLP Project. And on July 31 and August 1, 2003, I attended the meeting for 300mm Wafer Project Review.

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature 林源斌 Ben Lin

Date 9/13/06

Affidavit of Facts

I, Jalex Sun (孫文彬) , am a Technical Manger of ACE (Advanced Chip Engineering Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No.65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu, Taiwan, R.O.C.

I hereby attest that, in Year 2003, I was responsible for material approval and process development in RD Project. And on July 3 and August 1, 2003, I attended the meeting for 300mm Wafer Project Review.

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature 孫文彬 jalex sun

Date 9/13 2006

Affidavit of Facts

I, Yatzu Wu (吳雅慈) , am a Product Manger of ACE (Advanced Chip Engineering Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No.65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu, Taiwan, R.O.C.

I hereby attest that, on July 31 and August 1, 2003, I took part in the RD Project Review Meeting that WK Yang chaired. The recorder was Bob. I was in charge of testing and verifying the process for 300mm Wafer Project.

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature 吳雅慈 Yatzu Wu

Date 2006/09/15

Affidavit of Facts

I, Liching Huang (黃麗卿) , am a RD engineer of ACE (Advanced Chip Engineering Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No.65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu, Taiwan, R.O.C.

I hereby attest that, on July 31 and August 1, 2003, I didn't attend the RD Project Review Meeting that WK Yang chaired. After meeting, I received the minutes.

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature 黃麗卿 Liching Huang

Date 9/13'06

育霈科技股份有限公司
Advanced Chip Engineering Technology Inc.

離職證明書
Resignation Certification

姓　名 Name	王誌榮 David Wang	出生日期 Date of Birth	民國51年05月25日 25-May-62
身份證字號 I.D. No	T120981941	性　別 Sex	男 Male
服務部門 Department	測試工程開發處 Testing Engineering Development Div.	職　稱 Job Title	總工程師 Fellow
到職日 Date of Employment	民國89年06月19日 19-Jun-00	離職日 Date of Leaving	民國93年11月19日 19-Qct-04
備　註 Remark	空白 Nil		

上述各項屬實，特此證明。
This is to certify that the above statements are true and correct.

人力資源部
Human Resources Department

育霈科技股份有限公司 人事專用章 新竹縣湖口鄉光復北路65號

中華民國九十五年八月十四日
Date：August 14, 2006

地址：新竹縣303新竹工業區光復北路六十五號　電話:03-5983232
Add： No.26, Kuang-Fu North Rd., Hsin-Chu Industrial Park, Hsin-Chu 303, Taiwan, R.O.C.
TEL：886-03-5983232　FAX：886-5986565

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Advanced Chip Engineering Technology Inc.

離職證明書
Resignation Certification

姓　名 Name	周玲如 Eva Chou	出生日期 Date of Birth	民國59年01月22日 22-Jan-70
身份證字號 I.D. No	J220173854	性　別 Sex	女 Female
服務部門 Department	先進技術研發處 Advanced Technology Div.	職　稱 Job Title	技術經理 Technical Manager
到職日 Date of Employment	民國89年04月17日 17-Apr-00	離職日 Date of Leaving	民國95年07月28日 28-Jul-06
備　註 Remark	空白 Nil		

上述各項屬實，特此證明。
This is to certify that the above statements are true and correct.

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Human Resources Department

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育霈科技股份有限公司
Advanced Chip Engineering Technology Inc.

離職證明書
Resignation Certification

姓　名 Name	陳昊天 Alex Chen	出生日期 Date of Birth	民國61年07月28日 28-Jul-72
身份證字號 I.D. No	G120620845	性　別 Sex	男 Male
服務部門 Department	測試工程部 Testing Engineering Dept.	職　稱 Job Title	經理 Manager
到職日 Date of Employment	民國89年04月21日 21-Apr-00	離職日 Date of Leaving	民國94年05月06日 06-May-05
備　註 Remark	空白 Nil		

述各項屬實，特此證明。
This is to certify that the above statements are true and correct.

人力資源部
Human Resources Department

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育霈科技股份有限公司
Advanced Chip Engineering Technology Inc.

離職證明書
Resignation Certification

姓　名 Name	龍俊均 Alex Long	出生日期 Date of Birth	民國65年08月30日 30-Aug-76
身份證字號 I.D. No	D122681683	性　別 Sex	男 Male
服務部門 Department	研發二處 R&D II Div.	職　稱 Job Title	副工程師 Assistant Engineer
到職日 Date of Employment	民國90年06月04日 04-Jun-01	離職日 Date of Leaving	民國92年08月14日 14-Aug-03
備　註 Remark	空白 Nil		

上述各項屬實，特此證明。
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Human Resources Department

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中華民國九十五年八月十一日
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育霈科技股份有限公司
Advanced Chip Engineering Technology Inc.

離職證明書
Resignation Certification

姓　名 Name	牟慶聰 Eddy Mou	出生日期 Date of Birth	民國51年09月20日 20-Sep-62
身份證字號 I.D. No	L121816080	性　別 Sex	男 Male
服務部門 Department	總經理室 President Office	職　稱 Job Title	副總經理 Vice President
到職日 Date of Employment	民國89年05月01日 01-May-00	離職日 Date of Leaving	民國93年09月30日 30-Sep-04
備　註 Remark	空白 Nil		

述各項屬實，特此證明。

This is to certify that the above statements are true and correct.

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育霈科技股份有限公司
Advanced Chip Engineering Technology Inc.

離職證明書
Resignation Certification

姓　名 Name	洪乾耀 Yao Hung	出生日期 Date of Birth	民國57年10月06日 06-Qct-68
身份證字號 I.D. No	R121714791	性　別 Sex	男 Male
服務部門 Department	製造處 Manufacturing Div.	職　稱 Job Title	資深處長 Senior Director
到職日 Date of Employment	民國89年03月01日 01-Mar-00	離職日 Date of Leaving	民國93年07月16日 18-Jul-04
備　註 Remark	空白 Nil		

上述各項屬實，特此證明。
This is to certify that the above statements are true and correct.

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Human Resources Department

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6 - 6

Meeting Minutes of 300mm wafer - Equipments
Date: 8/8/2003
Place: 503 room
Attend: WK, Yao, Ben, Ye, Jalex

Summary and Actions:

- To discuss with vendor for design and making pick & place of 300mm wafer w/ flip the chip, 9" tray size
  - Direct to pick the chip and place into "tool" for 200mm size
  - W/flip the chip function (face down - circuit side down)
  - W/9" tooling size (tray) function & loading / off-loading function
  - W/input wafer (saw) up to 300mm size
- To design the equipment and tooling for glass "taping"
  - W/Z direction step motor function
  - W/vacuum hold the chip into "cavity tool" function
  - W/vacuum hold the "glass" for taping
  - W/taping sensor for protection
- To design the "ACE stepper" by using the following functions of equipment
  - Auto prober (TSK) w/programming X/Y/Z/Thilta, w/vacuum chuck
  - Patten recognition function for fine alignment.
  - Light source and control for photo development

  The machine can do the single step and multi-die step photo developing.

  The target cost is under NT10kk.

-To modify the current "點膠機" for cutting the 200mm "Glass" from square to round type w/flat

-RD I need to define the thickness of glass on 8/12 for process development.

The next meeting will be 2PM on 8/15.

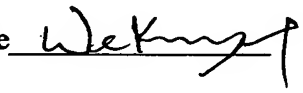
WK

Affidavit of Facts

I, Wen-kun Yang (楊文焜), am a C.E.O of ACE (Advanced Chip Engineering Technology Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No. 65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu 303, Taiwan, R.O.C.

I hereby attest that, on August 8, 2003, I have held the meeting to discuss the equipment issue for handling the 300mm wafer (panel), the members of group meeting are Yao who is the manufacturing leader and Ben who is the equipment leader and Ye who is the production supervisor and Jalex who is the process leader. The meeting minutes is the summary and action items。

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature 

Date Sept. 11, 2006

Affidavit of Facts

I, Ben Lin(林源斌) , am a Assistant Manger of ACE (Advanced Chip Engineering Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No.65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu, Taiwan, R.O.C.

I hereby attest that, on August 8, 2003, I attended the meeting for the equipment design of 300mm wafer. I was the leader of equipment department and responsible for the equipment surveying.

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature Ben Lin 林源斌

Date 9/13/06.

Affidavit of Facts

I, Jalex Sun (孫文彬) , am a Technical Manger of ACE (Advanced Chip Engineering Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No.65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu, Taiwan, R.O.C.

I hereby attest that, in Year 2003, I was responsible for material approval and process development in 300MM wafer project. And on August 8, 2003, I attended the meeting to discuss the equipment issue. The meeting minutes is the summary and action items.

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature 孫文彬 Jalex Sun

Date 9/3 2006

育霈科技股份有限公司
Advanced Chip Engineering Technology Inc.

離職證明書
Resignation Certification

姓　名 Name	洪乾耀 Yao Hung	出生日期 Date of Birth	民國57年10月06日 06-Qct-68
身份證字號 I.D. No	R121714791	性　別 Sex	男 Male
服務部門 Department	製造處 Manufacturing Div.	職　稱 Job Title	資深處長 Senior Director
到職日 Date of Employment	民國89年03月01日 01-Mar-00	離職日 Date of Leaving	民國93年07月16日 18-Jul-04
備　註 Remark	空白 Nil		

上述各項屬實，特此證明。
This is to certify that the above statements are true and correct.

人力資源部
Human Resources Department

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6 - 7

300mm wafer handling case:

Date: 9/22/2003

1. 300mm wafer Back-lapping
   - 甲、Thickness: 300u
   - 乙、Wafer mount into Al frame with blue tape
   - 丙、Shipping the blue tape wafer to ACET
   - 丁、ACET return the Al frame back to PTI after saw

2. 300mm wafer Back-lapping + Saw the wafer to 4pcs (1/4 圓)
   - 甲、Thickness: 300u
   - 乙、Wafer mount into Al frame with blue tape
   - 丙、Saw the wafer to 4pcs (切成 4 片 4/1 圓)
   - 丁、Ship the blue tape wafer to ACET
   - 戊、ACET return the Al frame after de-taping the wafer.

3. 300mm wafer Back-lapping + saw the wafer + pick & place the good dies into tray or 200mm blue tape.
   - 甲、Thickness: 300u
   - 乙、Wafer mount into Al frame with blue tape
   - 丙、Saw the wafer to individual dies
   - 丁、Pick & place the good dies into tray or 200mm blue tape form
   - 戊、Ship the Tray w/good dies or 200mm blue tape dies to ACET
   - 己、ACET return the Tray or 200mm Al frame back to PTI.

Materials Flow :

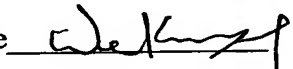
PSC ship the wafer to PTI for back-lapping +(and/or Saw, P&P) service
PTI ship the processed wafer/dies to ACET
ACET return the "tools" back to PTI
PTI send the "Invoice" with materials to ACET
PSC offer the "wafer mapping" data for good dies pick.

Affidavit of Facts

I, Wen-kun Yang (楊文焜), am a C.E.O of ACE (Advanced Chip Engineering Technology Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No. 65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu 303, Taiwan, R.O.C.

I hereby attest that, on September 22, 2003, I have created the memo. As 300mm wafer handling case to describe the handling procedure and material flow of 300mm wafer project. At that time, I am helping the project development, too.

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature 

Date Sept. 11, 2006

6 - 8

	process name	material	equipment	question	action	member	date
	laser cutting glass	glass	laser cutting	不能有切邊	利用雷射切割notch	林源斌	
	cleanning glass	acetone/IPA/DI water/N2	manual clean			林志偉	
	printting UV curing dice attach	KJC-7805X-7-4	manual printer	thinkness is not enough	請原廠提供更高黏度之產品	林志偉	
	dispensingThermal Conductivity paste	XE4450	dispenser	如果熱阻太高時	增加導熱膠	孫文彬	
	dice pick up & place manual tooling made	SU-8	manual coater	SU-8與鋁板附著力太弱.顯影後尺寸縮小	調整參數	孫文彬	
	dice pick up & place auto tooling made	SU-8	manual coater	廠內無法sputter Ti/Cu	委外製作	林源斌	
	dice pick up & place		manual tooling			林志偉	
	UV exposure		大祥曝光機			林志偉	
	cleanning substract	acetone/IPA/N2	manual clean			林志偉	
新增站別	printting fill paste	Q1-9239	auto printer (EKRA-X5)	溢膠	調整參數	陳銘賢 陳明勛	
	oven curing		OVEN			陳銘賢 陳明勛	
	rie cleanning	O2+CF4	RIE			林明輝	
	coating Dielectric Layer	SINR3170-3&SINR3170-L18&BCB	manual coater			吳雅慧 周昭男	
	softbak Dielectric Layer		OVEN			吳雅慧 周昭男	
	exposure Dielectric Layer		ALIGNER			吳雅慧 周昭男	
	prebak Dielectric Layer		OVEN			吳雅慧 周昭男	
	develop Dielectric Layer	IPA	manual develop	顯影後有下列情形 1.剝離2.顯影未淨3.形狀不良	調整參數	吳雅慧 周昭男	
	Dielectric Layer Post Cure		OVEN			吳雅慧 周昭男	
	Dielectric Layer RIE Descum		RIE			林明輝	
	Sputtering	Ti/Cu	SPUTTER			林明輝	
	PR Coating	TOK P-900	SUSS coater			林明輝 吳雅慧	
	PR Exposure		ALIGNER			林明輝 吳雅慧	
	PR Develop	P7-G	SUSS coater	邊緣顯影不良	調整參數	林明輝 王國威	
	PR RIE Ashing	依產線現有程序	依產線現有程序			林明輝	
	Cu Plating	依產線現有程序	依產線現有程序			吳泓均	
	QDR Clean3	依產線現有程序	依產線現有程序			吳泓均	
	Ni Plating	依產線現有程序	依產線現有程序			吳泓均	
	QDR Clean4	依產線現有程序	依產線現有程序			吳泓均	
	Au Plating	依產線現有程序	依產線現有程序			吳泓均	
	QDR Clean5	依產線現有程序	依產線現有程序			吳泓均	
	Plated Drying	依產線現有程序	依產線現有程序			吳泓均	
	Au Plating IPQC	依產線現有程序	依產線現有程序			吳泓均	
	PR Stripping1	依產線現有程序	依產線現有程序			吳泓均	
	PR Stripping2	依產線現有程序	依產線現有程序			吳泓均	
	PR Stripping3	依產線現有程序	依產線現有程序			吳泓均	
	QDR Clean6	依產線現有程序	依產線現有程序			吳泓均	
	Stripped Drying	依產線現有程序	依產線現有程序			吳泓均	
	Stripped IPQC	依產線現有程序	依產線現有程序			吳泓均	
	Stripped RIE Clean	依產線現有程序	依產線現有程序			吳泓均	
	Stripped RIE Clean IPQC	依產線現有程序	依產線現有程序			吳泓均	
	Cu Etching	依產線現有程序	依產線現有程序			吳泓均	
	QDR Clean7	依產線現有程序	依產線現有程序			吳泓均	
	Ti Etching	依產線現有程序	依產線現有程序			吳泓均	
	QDR Clean8	依產線現有程序	依產線現有程序			吳泓均	
	Ti Etching Drying	依產線現有程序	依產線現有程序			吳泓均	
	Ti Etching IPQC	依產線現有程序	依產線現有程序			吳泓均	
	Pre-solder Mask Baking	依產線現有程序	依產線現有程序			吳泓均	
	Solder Mask Printing	依產線現有程序	依產線現有程序			陳銘賢 陳明勛	
	Solder Mask Printing IPQC	依產線現有程序	依產線現有程序			陳銘賢 陳明勛	
	Solder Mask Pre-Baking	依產線現有程序	依產線現有程序			陳銘賢 陳明勛	
	Solder Mask Exposure	依產線現有程序	依產線現有程序			陳銘賢 陳明勛	
	Solder Mask Develop	依產線現有程序	依產線現有程序			陳銘賢 陳明勛	
	Solder Mask Develop IPQC	依產線現有程序	依產線現有程序			陳銘賢 陳明勛	
	Solder Mask Post Cure	依產線現有程序	依產線現有程序			陳銘賢 陳明勛	
	Solder Mask Post Cure IPQC	依產線現有程序	依產線現有程序			陳銘賢 陳明勛	
	Solder Mask UV Cure	依產線現有程序	依產線現有程序			陳銘賢 陳明勛	
	Back Side primer paint printing	白漆	auto printer (EKRA-X5)	白漆印刷厚度需考慮		陳銘賢 陳明勛	
	Back Side primer paint cure		oven			陳銘賢 陳明勛	

Back Side Marking Printing	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Back Side Marking Printing IPQC	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Back Side Marking Pre-Baking	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Back Side Marking Exposure	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Back Side Marking Develop	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Back Side Marking Develop IPQC	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Back Side Marking Post Cure	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Back Side Marking Post Cure IPQC	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Pre-ball Placement RIE Clean1	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Pre-ball Placement IPQC	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Flux Printing	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Ball Placement	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Reflow	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Ball Placement IPQC	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Flux Cleaning	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Flux Cleaned Drying	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Flux Cleaned Baking	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Flux Cleaning IPQC	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Final Test			
Wafer Mounter			
Wafer Mounter IPQC			
Wafer Dicing			
Wafer Dicing IPQC			
UV			
UV IPQC			
Chip Sorter			
Chip Sorter IPQC			
EQ test			
Ball inspection			
Packing			
Packing IPQC			
OQC			

Before we go further on this project, i would like to have more input from your side. Please advice on the following issues :-

PROCESS /EQUIPMENT:-

1. What's the resist uniformity on the wafer?
2. Die size?
3. Size of mask/ mask holder?
4. What's the Via opening for each die/specs?
5. What's the intensity needed/ wavelength?
6. For TSK prober, please provide details desription of the machine/ manual if possible?
7. What's the minimum step (1um,2um etc)in X,Y & Z?
8. On TSK how to level the wafer to mask (Suss use WEC)?
9. Can we program different gap (Alignment/Exposure gap)?
10. What software is TSK using ? Need to know so we can integrate the shuttler control in the Lamphouse.

Affidavit of Facts

I, Jalex Sun (孫文彬) , am a Technical Manger of ACE (Advanced Chip Engineering Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No.65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu, Taiwan, R.O.C.

I hereby attest that, in Year 2003, I was responsible for material approval and process development in 300MM wafer project. And on September 29, 2003, I listed a table for the process control.

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature 孫文彬 Jalex Sun

Date 9/13 2006

Doc No	File (File Date)	Date	Testimony of Custodian or Qualified Witness
7-1	12TO8_A_FT.DOC 2003.10.6	Oct. 3rd, 2003	
	12轉8 SIMULATION.PPT 2003.10.9	Oct. 9th, 2003	File Author: National Tsing Hua University
7-2	300MM WAFER FOR WL-CSP TRI.XLS	Oct. 16th-17th, 2003	Leader: David Lin、David Wang、Ben Lin
7-3	12.DOC 2003.10.29	Oct. 29th, 2003	File Author: Wen-kun Yang
7-4	WAFER LEVEL PACKAGING.PPT 200310.31	Oct. 31st, 2003	File Author: Wen-kun Yang
7-5	RDMEETING MINUTES ON 1106.DOC 2003.11.7	Nov. 7th, 2003	File Author: Wen-kun Yang

7 - 1

PSC 300mm 0.13u DDR WL-CSP package performance
First test result by using the linked dice of 0.13u

Please find the FT test @ 80C for PSC 12" to 8" #03 wafer result in the attatched files.
(a12to803.asc is the 8-DUTs result ; a12to803.asc is the 1-DUT result ; b12to803.asc.cmp is the compare file)
And according to the compare file, it seems 8-DUTs P/C testing have no big problem.

For your reference.


b12to803.asc.cmp


a12to803.asc


b12to803.asc

Probe Card: 8 DUT, @80c testing summary
TEST TIME = 0000 0018 0042
##
FT1 Summary Report
Date :03/10/03
Time :10:59:35
Device Type :PSC 32MX8 DDR
PGM NAME :T256DFXN
LOT NO :12TO8
WaferId :03
TESTER NO :T8202
P/C NO :
OPER.NO :A277
##

BIN	COUNT	YIELD %
UNITS TESTED	360	
UNITS PASS	5	1 %
BIN 0 PASS-500 CL=2.5	5	1 %
BIN 9 PASS-433 CL=2.0	0	0 %
BIN 1 PASS-400 CL=2.5	0	0 %
BIN 2 PASS-333 CL=2.5	0	0 %
BIN 3 PASS-400 CL=2.0	0	0 %
BIN 5 GROSSFUNCTION FAIL	218	60 %
BIN 6 REFRESH FAIL	0	0 %
BIN 6 SPEED FAIL	0	0 %
BIN 7 LEAKAGE FAIL	23	6 %

##
FT1 Wafer mapping Report
##

7858
8575885
855585885
5585558855
55587558585
755875575858
5855855558555
55885555555855
55555557558585
785885585555855
857885585855555
5555559857558888
5558585588555588
8885855575557588
5088558555887058
5555585555557588
8755855885557588
55855555755505 58
858555558555585
555558558555850
88555558555505
58585557585588
5555578585555
585558788585
85875855555
5875558855
888888885
8588858
8887

Probe Card: 1 DUT, @80c Testing summary
TEST TIME = 0000 0024 0058
##
EQ1 Summary Report
Date :03/10/02
Time :14:13:47
Device Type :PSC 32MX8 DDR
PGM NAME :T256DEQA
LOT NO :12TO8
WaferId :03
TESTER NO :T8207
P/C NO :1
OPER.NO :1
##

BIN	COUNT	YIELD %
UNITS TESTED	360	
UNITS PASS	4	1 %
BIN 1 PASS G/F	4	1 %
BIN 2 N/A	0	0 %
BIN 3 N/A	0	0 %
BIN 4 N/A	0	0 %
BIN 5 G/F FAIL	218	60 %
BIN 6 N/A	0	0 %
BIN 7 LEAKAGE FAIL	23	6 %
BIN 8 CONTINU FAIL	115	31 %

Station 1 Summary Report Finished !!
Wafer Flat is RIGHT side

##
EQ1 Wafer mapping Report
##

7858
8575885
855585885
5585558855
55587558585
755875575858
5855855558555
55885555555855
55555557558585
7858855855555855
8578855858555555
5555555857558888
5558585588555588
8885855575557588
5588558555887158
5555585555557588
8755853885557588
8585555575551558
858555558555585
555558558555851
88555558555515
58585557585588
5555578585555
585558788585
85875855555
5875558855
888888885
8588858
8887

It works!!

I am sampling test some EQ test PASS dies.
These dies could also PASS the SPEED TEST on the 8-DUT P/C @80C.
The shmoo data is as following.
And it seems faster than the 8" PSC device.

For your referance.

B. Regards,

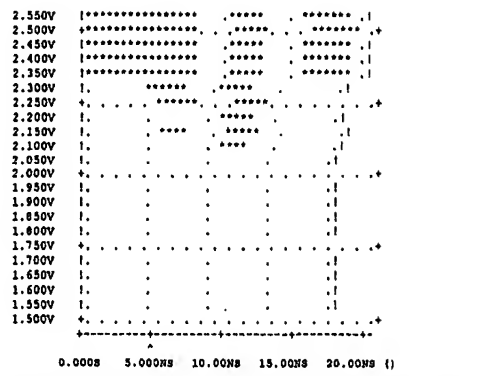
12" To 8" PSC Shmoo

```
***** 2D-SHMOO *****                                    SHM2  REV.03
DATE:  2003/10/02  TEST: 280
SAMPLE#: 1441              SHMOO#:                  DUT#: 10
DEVICE:                    LOT#:
COND:                                          FUNC: MPAT P256DDRD
FUNC: PC(MAIN) #00000040     FUNC: PC(SUB)  #00000040
X-AXIS:                    STRB1                  X-DELT= 500.0PS
Y-AXIS:                    VS1                    Y-DELT=-100.0MV

      0.000S    5.000NS   10.00NS   15.00NS   20.00NS   25.00NS ()
()          V
       +---------+---------+---------+---------+---------+-
3.000V  +********** . .****** . . ******* . ******* . . ***+
2.900V  |**********   ******    *******  *******    ***|
2.800V >|**********   ******    *******  *******    ***|<
2.700V  |**********   ******    *******  ******     ***|
2.600V  |**********   ******     ******  *****     ***|
2.500V  +********** . . ****. . . .****** . .*****. . . ***+
2.400V  |**********   *****     *****    *****      **|
2.300V  |.*********   ****.     *****    *****      **|
2.200V  |.       .       .       .       .       .|
2.100V  |.       .       .       .       .       .|
2.000V  +. . . . . . . . . . . . . . . . . . . . . . .+
1.900V  |.       .       .       .       .       .|
1.800V  |.       .       .       .       .       .|
1.700V  |.       .       .       .       .       .|
1.600V  |.       .       .       .       .       .|
1.500V  +. . . . . . . . . . . . . . . . . . . . . . .+
       +---------+---------+---------+---------+---------+-
            ^
      0.000S    5.000NS   10.00NS   15.00NS   20.00NS   25.00NS ()
```

```
***** 2D-SHMOO *****                                    SHM2  REV.03
DATE:  2003/10/02  TEST: 280
SAMPLE#: 1441              SHMOO#:                  DUT#: 16
DEVICE:                    LOT#:
COND:                                          FUNC: MPAT P256DDRD
FUNC: PC(MAIN) #00000040     FUNC: PC(SUB)  #00000040
X-AXIS:                    STRB1                  X-DELT= 500.0PS
Y-AXIS:                    VS1                    Y-DELT=-100.0MV

      0.000S    5.000NS   10.00NS   15.00NS   20.00NS   25.00NS ()
()          V
       +---------+---------+---------+---------+---------+-
3.000V  +********** . .****** . . ******. . ******. . .****+
2.900V  |**********.  ******   ******   ******    ****|
2.800V >|**********.  ******   ******   ******    ****|<
2.700V  |**********.  ******   ******   ******    ****|
2.600V  |**********.  *****.   ******   ******     ***|
2.500V  +**********. . .*****. . . .*****. . .*****. . . ***+
2.400V  |**********.   ****.    *****    *****     ***|
2.300V  |.  *******.   ****.    *****    *****     ***|
2.200V  |.       .       .       .       .       .|
2.100V  |.       .       .       .       .       .|
2.000V  +. . . . . . . . . . . . . . . . . . . . . . .+
1.900V  |.       .       .       .       .       .|
1.800V  |.       .       .       .       .       .|
1.700V  |.       .       .       .       .       .|
1.600V  |.       .       .       .       .       .|
1.500V  +. . . . . . . . . . . . . . . . . . . . . . .+
       +---------+---------+---------+---------+---------+-
            ^
      0.000S    5.000NS   10.00NS   15.00NS   20.00NS   25.00NS ()

     FILE NAME : C0016280
```

8" PSC Shmoo

```
***** 2D-SHMOO *****                                    SHM2  REV.03
DATE:  2003/09/25  TEST: 315
SAMPLE#: 0                 SHMOO#:                  DUT#: 2
DEVICE: 32MX8 DDR          LOT#:
COND:                                          FUNC: MPAT P256TMPX
FUNC: PC(MAIN) #00000040     FUNC: PC(SUB)  #00000040
X-AXIS:                    STRB1                  X-DELT= 500.0PS
Y-AXIS:                    VS1                    Y-DELT=-50.00MV

      0.000S    5.000NS   10.00NS   15.00NS   20.00NS ()
()          V
       +---------+---------+---------+---------+-
```

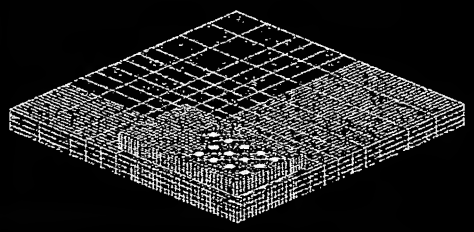

2.550V
2.500V
2.450V
2.400V
2.350V
2.300V
2.250V
2.200V
2.150V
2.100V
2.050V
2.000V
1.950V
1.900V
1.850V
1.800V
1.750V
1.700V
1.650V
1.600V
1.550V
1.500V
0.000S
5.000NS
10.00NS
15.00NS
20.00NS

Main assumptions

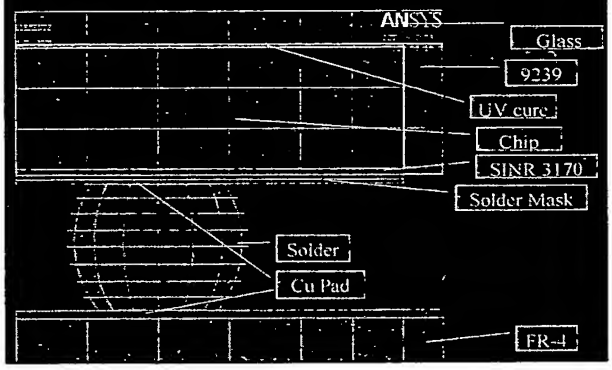
- No initial residual stress is considered.
- Perfect bonding is assumed at all interfaces between different materials and no void exists in the solder ball.
- All the material properties of the components, except the solder ball, are assumed to be linear-elastic, homogenous, isotropic, and temperature-independent over the temperature range considered.
- Uniform thermal loading, steady state solution, stress free is assumed as room temperature.

Model global view

- For dual axial symmetry ⇨ build ¼ model



Model local view



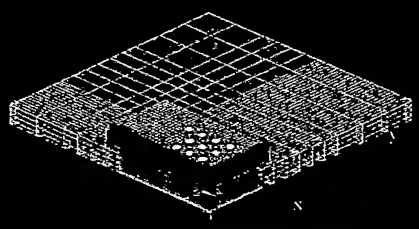
Material properties

Key Dimensions

- Chip Size:5.77 * 10.38 * 0.3 (mm)
- Glass thickness:0.55mm
- UV cure thickness:0.01mm
- SINR 3170 thickness:0.015mm
- Solder Mask of PCB:0.02mm

Boundary Condition

- Temperature cycling:-55~125 C



Strain Distribution(Real Ball)

Life cycle(Real ball)

Equivalent plastic strain range:0.013692

Life cycles:1980

7 - 2

FO-WLP – Project development
1st sample making Date

Year 2003

站名	material	開始時間		leader	
glass baking		10/16/am:9:00			
dice pick up & place	KJC-7805X-7-4	10/16/pm:8:00	林志偉	林明輝	
printting fill paste	Q1-9239	10/16/pm:10:00	陳銘賢	林明輝	
coating Dielectric Layer	SINR3170-L10	10/17/am:03:00	周昭男	林明輝	3pic mask Al pad
Sputtering		10/17/am:09:00	林明輝	林明輝	
PR Coating		10/17/am:10:30	吳雅慧	林明輝	
plating		10/17/pm:01:10	林淑貞	林明輝	
PR Stripping			林淑貞	林明輝	
Cu Etching			林淑貞	林明輝	
Ti Etching			林淑貞	林明輝	
Solder Mask Printing		10/17/pm:05:00	陳銘賢	林明輝	
Back Side Marking Printing		10/17/pm:07:00	陳銘賢	林明輝	
Ball Placement		10/17/pm:09:00	陳銘賢	林明輝	
Final Test		10/17/pm:11:00	陳昊天	david	
dice saw			曾明寶	林源斌	
chip sort			邱俊益	林源斌	
chip oqc			許獻文	david	
sort			leo	david	

Probe Card: 8 DUT, @80c testing summary
TEST TIME = 0000 0018 0042

##########

FT1 Summary Report
Date : 03/10/03
Time : 10:59:35
Device Type: PSC 32MX8 DDR
PGM NAME: T256DFXN
LOT NO: 12TO8
WaferId : 03
TESTER NO: T8202
P/C NO:
OPER NO: A277

##########

BIN	COUNT	YIELD%
UNITS TESTED	360	
UNITS PASS	5	1%
BIN 0 PASS-500 CL=2.5	5	1%
BIN 9 PASS-433 CL=2.0	0	0%
BIN 1 PASS-400 CL=2.5	0	0%
BIN 2 PASS-333 CL=2.5	0	0%
BIN 3 PASS-400 CL=2.0	0	0%
BIN 5 GROSSFUNCTION FAIL	218	60%
BIN 6 REFRESH FAIL	0	0%
BIN 6 SPEED FAIL	0	0%
BIN 7 LEAKAGE FAIL	23	6%
BIN 8 CONTINU FAIL	114	31%

Station 2 Summary Report Finished!!

GEIL

Oct. 20th, 2003

File : 300mm Wafer For WL-CSP TR1.

站名	material	開始時間		leader	
glass baking		10/16/am:09:00			
dice pick up & place	KJC-7805X-7-4	10/17/pm:05:00	林志偉	林明輝	
printting fill paste	Q1-9239	10/17/pm:07:00	陳銘賢	林明輝	
coating Dielectric Layer	SINR3170-L18	10/17/pm:10:00	周昭男	林明輝	3pic mask Al pad刮傷
Sputtering		10/18/am:02:00	林明輝	林明輝	
PR Coating	改用geil mask	10/18/am:04:00	吳雅慈	林明輝	
plating		10/18/am:07:00	林淑真	林明輝	
PR Stripping			林淑真	林明輝	
Cu Etching			林淑真	林明輝	
Ti Etching			林淑真	林明輝	
Solder Mask Printing		10/18/am:11:00	陳銘賢	林明輝	
Back Side Marking Printing		10/18/pm:02:00	陳銘賢	林明輝	
Ball Placement		10/17/pm:04:00	陳銘賢	林明輝	
Final Test		10/17/pm:06:00	陳昊天	david	
dice saw			黃明寶	林源斌	
chip sort			邱俊益	林源斌	
chip oqc			許獻文	david	
smt			leo	david	

TWINMOS

站名	material	開始時間		leader	
glass baking		10/16/am:9:00			
dice pick up & place	KJC-7805X-7-4	10/16/pm:8:00	林志偉	林明輝	
printting fill paste	Q1-9239	10/16/pm:10:00	陳銘賢	林明輝	
coating Dielectric Layer	SINR3170-L18	10/17/am:03:00	周昭男	林明輝	3pic mask Al pad刮傷
Sputtering		10/17/am:09:00	林明輝	林明輝	
PR Coating		10/17/am:10:30	吳雅慈	林明輝	
plating		10/17/pm:01:10	林淑真	林明輝	
PR Stripping			林淑真	林明輝	
Cu Etching			林淑真	林明輝	
Ti Etching			林淑真	林明輝	
Solder Mask Printing		10/17/pm:05:00	陳銘賢	林明輝	
Back Side Marking Printing		10/17/pm:07:00	陳銘賢	林明輝	
Ball Placement		10/17/pm:09:00	陳銘賢	林明輝	
Final Test		10/17/pm:11:00	陳昊天	david	
dice saw			黃明寶	林源斌	
chip sort			邱俊益	林源斌	
chip oqc			許獻文	david	
smt			leo	david	

	process name	material	equipment	question	action	member	date
	laser cutting glass	glass	laser cutting	不能有切邊	利用雷射切割notch	林源斌	
	cleanning glass	acetone/IPA/DI water/N2	manual clean			林志偉	
	printting UV curing dice attach	KJC-7805X-7-4	manual printer	thinkness is not enough	請原廠提供更高黏度之產品	林志偉	
	dispensingThermal Conductivity paste	XE4450	dispenser	如果熱阻太高時	增加導熱膠	孫文彬	
	dice pick up & place manual tooling made	SU-8	manual coater	SU-8與鋁板附著力太弱,顯影後尺寸縮小	調整參數	孫文彬	
	dice pick up & place auto tooling made	SU-8	manual coater	廠內無法sputter Ti/Cu	委外製作	林源斌	
	dice pick up & place		manual tooling			林志偉	
	UV exposure		大祥曝光機			林志偉	
	cleanning substract	acetone/IPA/N2	manual clean			林志偉	
新增站別	printting fill paste	Q1-9239	auto printer (EKRA-X5)	溢膠	調整參數	陳銘賢 陳明勛	
	oven curing		OVEN			陳銘賢 陳明勛	
	rie cleanning	O2+CF4	RIE			林明輝	
	coating Dielectric Layer	SINR3170-3&SINR3170-L18&BCB	manual coater			吳雅慈 周昭男	
	softbak Dielectric Layer		OVEN			吳雅慈 周昭男	
	exposure Dielectric Layer		ALIGNER			吳雅慈 周昭男	
	prebak Dielectric Layer		OVEN			吳雅慈 周昭男	
	develop Dielectric Layer	IPA	manual develop	顯影後有下列情形 1.剝離2.顯影未淨3.形狀不良	調整參數	吳雅慈 周昭男	
	Dielectric Layer Post Cure		OVEN			吳雅慈 周昭男	
	Dielectric Layer RIE Descum		RIE			林明輝	
	Sputtering	Ti/Cu	SPUTTER			林明輝	
	PR Coating	TOK P-900	SUSS coater			林明輝 吳雅慈	
	PR Exposure		ALIGNER			林明輝 吳雅慈	
	PR Develop	P7-G	SUSS coater	邊緣顯影不良	調整參數	林明輝 王國威	
	PR RIE Ashing	依產線現有程序	依產線現有程序			林明輝	
	Cu Plating	依產線現有程序	依產線現有程序			吳泓均	
	QDR Clean3	依產線現有程序	依產線現有程序			吳泓均	
	Ni Plating	依產線現有程序	依產線現有程序			吳泓均	
	QDR Clean4	依產線現有程序	依產線現有程序			吳泓均	
	Au Plating	依產線現有程序	依產線現有程序			吳泓均	
	QDR Clean5	依產線現有程序	依產線現有程序			吳泓均	
	Plated Drying	依產線現有程序	依產線現有程序			吳泓均	
	Au Plating IPQC	依產線現有程序	依產線現有程序			吳泓均	
	PR Stripping1	依產線現有程序	依產線現有程序			吳泓均	
	PR Stripping2	依產線現有程序	依產線現有程序			吳泓均	
	PR Stripping3	依產線現有程序	依產線現有程序			吳泓均	
	QDR Clean6	依產線現有程序	依產線現有程序			吳泓均	
	Stripped Drying	依產線現有程序	依產線現有程序			吳泓均	
	Stripped IPQC	依產線現有程序	依產線現有程序			吳泓均	
	Stripped RIE Clean	依產線現有程序	依產線現有程序			吳泓均	
	Stripped RIE Clean IPQC	依產線現有程序	依產線現有程序			吳泓均	
	Cu Etching	依產線現有程序	依產線現有程序			吳泓均	
	QDR Clean7	依產線現有程序	依產線現有程序			吳泓均	
	Ti Etching	依產線現有程序	依產線現有程序			吳泓均	
	QDR Clean8	依產線現有程序	依產線現有程序			吳泓均	
	Ti Etching Drying	依產線現有程序	依產線現有程序			吳泓均	
	Ti Etching IPQC	依產線現有程序	依產線現有程序			吳泓均	
	Pre-solder Mask Baking	依產線現有程序	依產線現有程序			吳泓均	
	Solder Mask Printing	依產線現有程序	依產線現有程序			陳銘賢 陳明勛	
	Solder Mask Printing IPQC	依產線現有程序	依產線現有程序			陳銘賢 陳明勛	
	Solder Mask Pre-Baking	依產線現有程序	依產線現有程序			陳銘賢 陳明勛	
	Solder Mask Exposure	依產線現有程序	依產線現有程序			陳銘賢 陳明勛	
	Solder Mask Develop	依產線現有程序	依產線現有程序			陳銘賢 陳明勛	
	Solder Mask Develop IPQC	依產線現有程序	依產線現有程序			陳銘賢 陳明勛	
	Solder Mask Post Cure	依產線現有程序	依產線現有程序			陳銘賢 陳明勛	
	Solder Mask Post Cure IPQC	依產線現有程序	依產線現有程序			陳銘賢 陳明勛	
	Solder Mask UV Cure	依產線現有程序	依產線現有程序			陳銘賢 陳明勛	
	Back Side primer paint printing	白漆	auto printer (EKRA-X5)	白漆印刷厚度需考慮		陳銘賢 陳明勛	
	Back Side primer paint cure		oven			陳銘賢 陳明勛	

Back Side Marking Printing	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Back Side Marking Printing IPQC	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Back Side Marking Pre-Baking	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Back Side Marking Exposure	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Back Side Marking Develop	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Back Side Marking Develop IPQC	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Back Side Marking Post Cure	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Back Side Marking Post Cure IPQC	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Pre-ball Placement RIE Clean1	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Pre-ball Placement IPQC	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Flux Printing	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Ball Placement	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Reflow	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Ball Placement IPQC	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Flux Cleaning	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Flux Cleaned Drying	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Flux Cleaned Baking	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Flux Cleaning IPQC	依產線現有程序	依產線現有程序	陳銘賢 陳明勛
Final Test			
Wafer Mounter			
Wafer Mounter IPQC			
Wafer Dicing			
Wafer Dicing IPQC			
UV			
UV IPQC			
Chip Sorter			
Chip Sorter IPQC			
BQ test			
Ball inspection			
Packing			
Packing IPQC			
OQC			

站名	material	開始時間		leader	
glass baking		10/16/am:09:00			
dice pick up & place	KJC-7805X-7-4	10/17/pm:05:00	林志偉	林明輝	
printting fill paste	Q1-9239	10/17/pm:07:00	陳銘賢	林明輝	
coating Dielectric Layer	SINR3170-L18	10/17/pm:10:00	周昭男	林明輝	3pic mask Al pad刮傷
Sputtering		10/18/am:02:00	林明輝	林明輝	
PR Coating	改用geil mask	10/18/am:04:00	吳雅慈	林明輝	
plating		10/18/am:07:00	林淑真	林明輝	
PR Stripping			林淑真	林明輝	
Cu Etching			林淑真	林明輝	
Ti Etching			林淑真	林明輝	
Solder Mask Printing		10/18/am:11:00	陳銘賢	林明輝	
Back Side Marking Printing		10/18/pm:02:00	陳銘賢	林明輝	
Ball Placement		10/17/pm:04:00	陳銘賢	林明輝	
Final Test		10/17/pm:06:00	陳昊天	david	
dice saw			黃明寶	林源斌	
chip sort			邱俊益	林源斌	
chip oqc			許獻文	david	
smt			leo	david	

站名	material	開始時間		leader	
glass baking		10/16/am:9:00			
dice pick up & place	KJC-7805X-7-4	10/16/pm:8:00	林志偉	林明輝	
printting fill paste	Q1-9239	10/16/pm:10:00	陳銘賢	林明輝	
coating Dielectric Layer	SINR3170-L18	10/17/am:03:00	周昭男	林明輝	3pic mask Al pad刮傷
Sputtering		10/17/am:09:00	林明輝	林明輝	
PR Coating		10/17/am:10:30	吳雅慈	林明輝	
plating		10/17/pm:01:10	林淑真	林明輝	
PR Stripping			林淑真	林明輝	
Cu Etching			林淑真	林明輝	
Ti Etching			林淑真	林明輝	
Solder Mask Printing		10/17/pm:05:00	陳銘賢	林明輝	
Back Side Marking Printing		10/17/pm:07:00	陳銘賢	林明輝	
Ball Placement		10/17/pm:09:00	陳銘賢	林明輝	
Final Test		10/17/pm:11:00	陳昊天	david	
dice saw			黃明寶	林源斌	
chip sort			邱俊益	林源斌	
chip oqc			許獻文	david	
smt			leo	david	

Affidavit of Facts

I, Ben Lin(林源斌) , am a Assistant Manger of ACE (Advanced Chip Engineering Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No.65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu, Taiwan, R.O.C.

I hereby attest that, on October 16-17, 2003, I was be the leader for engineering and manpower coordination in 12" transfer to 8" FO-WLP Project. In GEIL and TwinMos projects, I was responsible for dice saw and chip sort.

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature 林源斌 Ben Lin 9/15/06

Date_____

育霈科技股份有限公司
Advanced Chip Engineering Technology Inc.

離職證明書
Resignation Certification

姓　名 Name	林明輝 David Lin	出生日期 Date of Birth	民國62年03月17日 30-Aug-76
身份證字號 I.D. No	K120404657	性　別 Sex	男 Male
服務部門 Department	製程工程處 Process Engineering Div.	職　稱 Job Title	技術副理 Technical Assistant Manager
到職日 Date of Employment	民國90年02月26日 26-Feb-01	離職日 Date of Leaving	民國94年11月30日 30-Nov-05
備　註 Remark	空白 Nil		

上述各項屬實，特此證明。
This is to certify that the above statements are true and correct.

人力資源部
Human Resources Department

育霈科技股份有限公司 人事專用章 新竹縣湖口鄉光復北路65號

中華民國九十五年八月十一日
Date：August 11, 2006

地址：新竹縣303新竹工業區光復北路六十五號　電話:03-5983232
Add： No.26, Kuang-Fu North Rd., Hsin-Chu Industrial Park, Hsin-Chu 303, Taiwan, R.O.C.
TEL：886-03-5983232　FAX：886-5986565

育霈科技股份有限公司
Advanced Chip Engineering Technology Inc.

離職證明書
Resignation Certification

姓　名 Name	王誌榮 David Wang	出生日期 Date of Birth	民國51年05月25日 25-May-62
身份證字號 I.D. No	T120981941	性　別 Sex	男 Male
服務部門 Department	測試工程開發處 Testing Engineering Development Div.	職　稱 Job Title	總工程師 Fellow
到職日 Date of Employment	民國89年06月19日 19-Jun-00	離職日 Date of Leaving	民國93年11月19日 19-Oct-04
備　註 Remark	空白 Nil		

上述各項屬實，特此證明。
This is to certify that the above statements are true and correct.

人力資源部
Human Resources Department

育霈科技股份有限公司 人事專用章 新竹縣湖口鄉光復北路65號

中華民國九十五年八月十四日
Date：August 14, 2006

地址：新竹縣303新竹工業區光復北路六十五號　電話:03-5983232
Add： No.26, Kuang-Fu North Rd., Hsin-Chu Industrial Park, Hsin-Chu 303, Taiwan, R.O.C.
TEL：886-03-5983232　FAX：886-5986565

7 - 3

12 -> 8 Project

Preparation for production:

- Materials qualification:
  - Glass: 平整度? 切圓? Notch? Available? [Ben - 10/31]
- BOM list: [Jalex - 10/29]
- Process recipe: [Yatza/David Lin - 10/29]
  - Glass saw: [Ben - 11/5]
  - Glass lapping for SO-DIMM [Jalex]
- Production Tools:
  - Glass mask: GEIL/ACE, Alignment keys? [Yao/David - 10/31]
  - Placement tools: TAT 1 day, Cost NT12k, by CNC [Jalex]
  - Printing tools: Okay
- Equipments:
  - P&P: [Yao - 10/30] PO by ACET
  - Glass bonding: review spec, PO, TAT=1m [Yao -
    - Review manual tooling?? [Yao - 10/30]
  - [stepper]
- Production flow: [Bob - 10/29]
- Run Card [Eva/Kenny - 10/30]
- Quality gate, inspection criteria [Eva - 10/30]
- Document: [Eva - 11/5]
- Training: [Yao - 11/5]
- Preliminary reliability: [Eva - 11/3]
  - PCT - 11/10
  - T/C -
- 2.2v dice for customers, 2.4v for reliability: [Eddy - 10/29]
- Al Pads experiment [Bob - 10/31]

Affidavit of Facts

I, Wen-kun Yang (楊文焜), am a C.E.O of ACE (Advanced Chip Engineering Technology Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No. 65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu 303, Taiwan, R.O.C.

I hereby attest that, on October 29, 2003, I have written the document "preparation for production" to descript the preparation of each items for 12" to 8" project (FO-WLP) to relative people of group, at that time, we are preparing the necessary work for production of FO-WLP in the short term period. ◦

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature 

Date Sept. 11, 2006

7 - 4

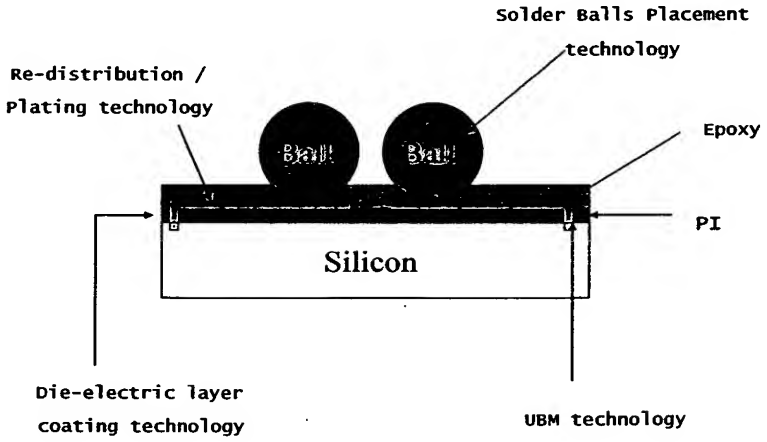
Wafer Level Packaging

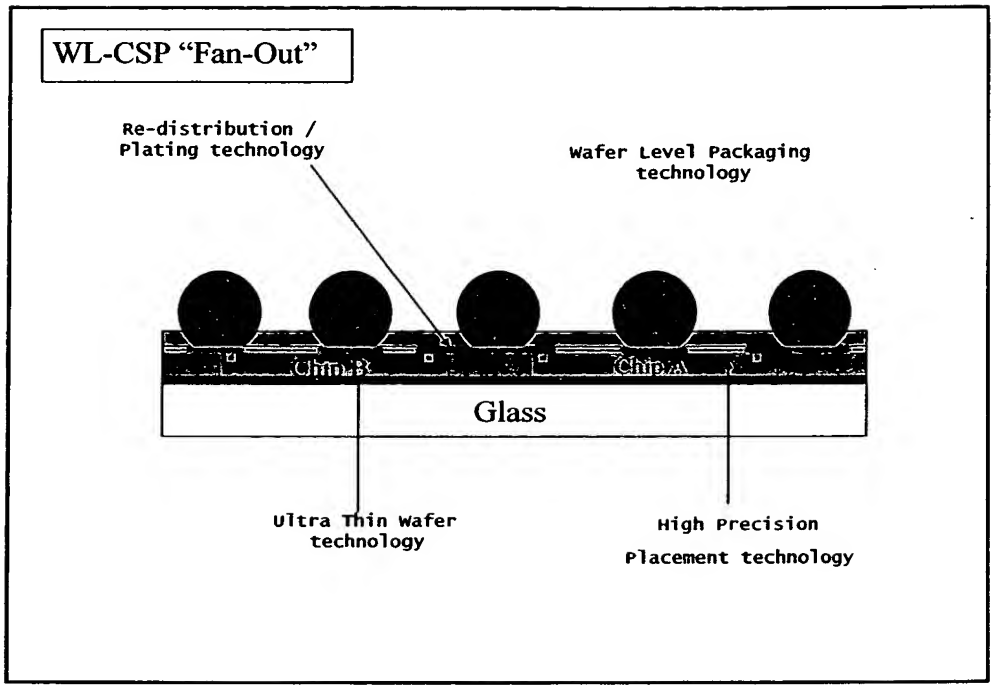
Basic Technologies

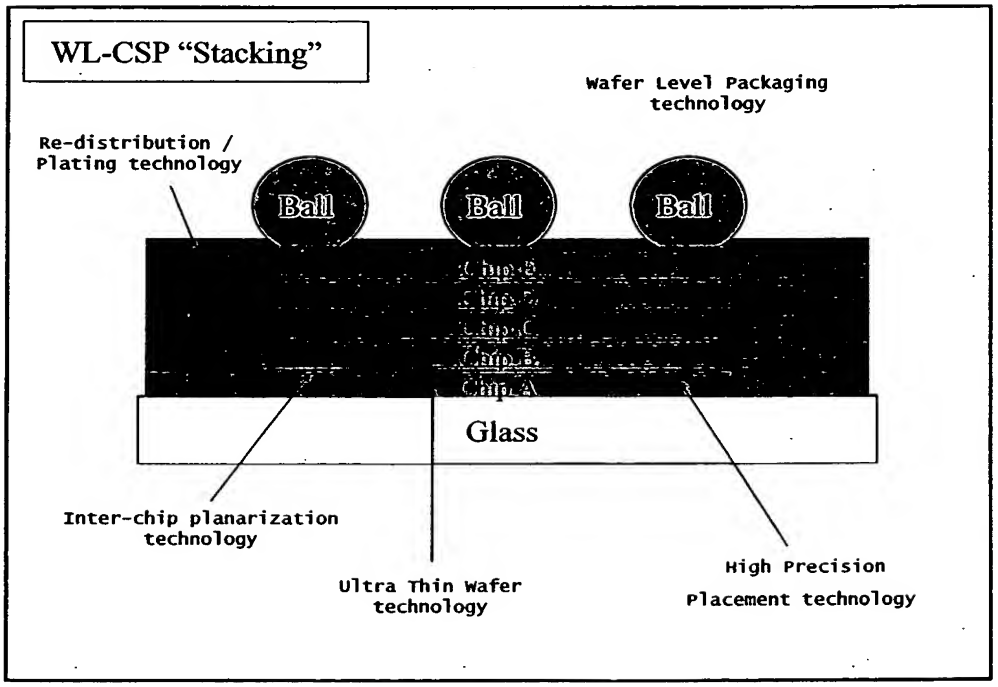
Advanced Chip Engineering Technology Inc.

Internal Use Only

WL-CSP "Fan-in"




WL-CSP "Fan-Out"
Re-distribution / Plating technology
Wafer Level Packaging technology
Chip B
Chip A
Glass
Ultra Thin Wafer technology
High Precision Placement technology


WL-CSP "Stacking"
Wafer Level Packaging technology
Re-distribution / Plating technology
Ball
Ball
Ball
Chip D
Chip C
Chip B
Chip A
Glass
Inter-chip planarization technology
Ultra Thin Wafer technology
High Precision Placement technology

Affidavit of Facts

I, Wen-kun Yang (楊文焜), am a C.E.O of ACE (Advanced Chip Engineering Technology Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No. 65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu 303, Taiwan, R.O.C.

I hereby attest that, on October 31, 2003, I have created the presentation file of Wafer Level Packaging that present the types of wafer level packaging including the fan-in and fan-out type etc. It is used for the internal discussion。

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature _____

Date Sept. 11, 2006

7 - 5

Meeting Minutes on 11/6 (RD Review) 4PM – 6PM

Current Project:

1. PSC
   - 甲、2.0G (project code: 9222)
     i. For ACET pin assignment
     ii. For GEIL pin assignment
   - 乙、2.5G (project code:)
     - JEDEC standard ball array 0.8mmx1.0mm pitch and body 8x13
2. NTC for 2.5G (project code:)
   - 甲、512Mb for JEDEC standard – verify the speed
   - 乙、256Mb for JEDEC standard – package qualification
3. ProMOS Project code:
   - 甲、2.0G - close due to engineering issue
   - 乙、2.5G for JEDEC standard
4. HighTech (dice form at tray – 300u thickness)
   - 甲、2.5G for 0.15u DDR (x8/x16) - waiting
5. Probe card for 2.5G @T5382A (1 DUT & 8 DUT)
6. Probe card for 2.0G @T5581P (1 DUT)
7. Probe card for 2.0G @T5382A (16 DUT) – pending
8. PC based tester
9. WL-CSP BIB for 2.0G – Pending (lower priority)
10. WL-CSP BIB for 2.5G – JEDEC standard: Waiting
11.

Summary:

1. SM group should issue the "New product request form" to cover the above project.
2. For NTC project: NTC should offer the document for both two types product within two day, the 512Mb product, ACET need to offer the engineering sample unit within 10 days. For 256Mb, NTC will take the package qualification procedure. ACET should handle it carefully.
3. For ProMOS project: ACET still in discussion with ProMOS, expect to get the result around a week. ACET prefer starting the UTT CSP then, ProMOS logo version later.
4. For 2.0G PSC project:
   - 甲、Identified the Glass materials and quality (Yao)

乙、Two set placement tools ready for production
丙、ACET version Glass mask will be ready on 11/10 (Bob)
丁、Expect the GEIL version glass mask will be ready on 11/18 (Bob)
戊、Glass based saw quality and outsource issue (Yao)
   i. To confirm it before 11/12 (Yao)
己、The possibility to lapping the Glass after WL process (Bob)
   i. SO-DIMM need the thickness same as 1.0G, if the glass lapping fail, then, we need to use the thin glass and thin dice for process during WLP.
      1. To find the Thin glass 300u (available & cost - Bob)
      2. To confirm the 200u wafer lapping cost (Yao)
      3. To overcome the automation during process issue (Yao)
      4. To do the drop test of module without cover (David/Eva)
庚、The alignment key issue verification should complete it before 11/14 (Yao)
辛、Need to solve the back lapping and saw, P&P issue in Nov. (Yao/WK)

5. For 2.5G PSC project: The first engineering sample will be ready on 11/11, WK need the mechanical sample for customers and news release.
6. Millie: Please assign the code number to group for cost control.
7. Probe card for 2.5G need to be ready on/before 11/11. (David)
8. Module test tools need to be ready on/before 11/11 (David)
9. Stop to order the BCB and relative materials that only for 8" wafer (MC)

Information: Pure 8" wafer from PSC may only 2000pcs for process in Nov. & Dec. ACET needs to focus on the 300mm and 2.5G standard package due to marketing concern.

- End of report -
- By WK Yang on 11/7

Affidavit of Facts

I, Wen-kun Yang (楊文焜), am a C.E.O of ACE (Advanced Chip Engineering Technology Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No. 65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu 303, Taiwan, R.O.C.

I hereby attest that, on November 6, 2003, I have held the RD review meeting to review the current project with staff, at that time, we have specified the 2.0G and 2.5G project that belongs to FO-WLP technology, we have done the samples and let the customers to evaluate。

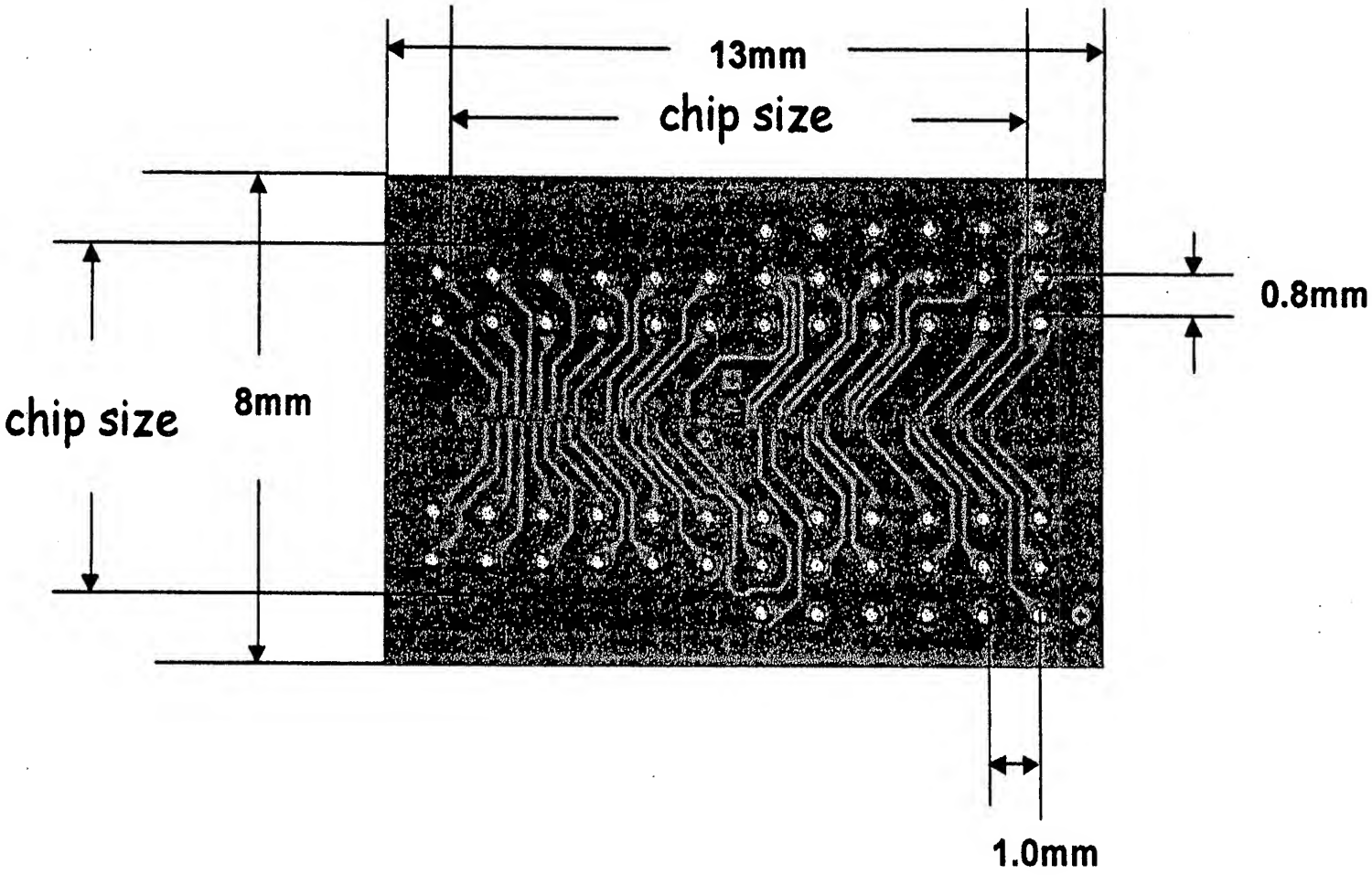
I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature 

Date Sept. 11, 2006

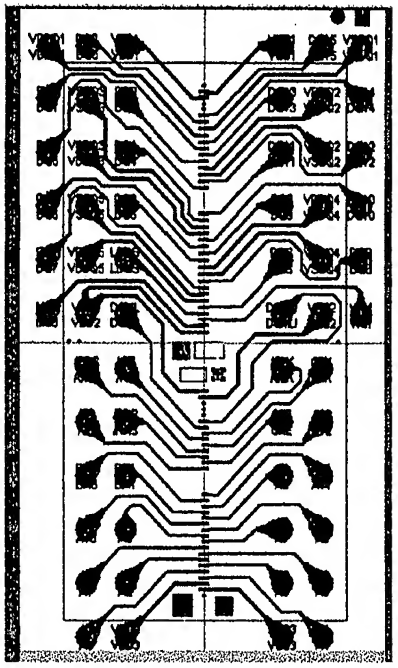
Doc No	File (File Date)	Date	Testimony of Custodian or Qualified Witness
8	掃瞄0004.JPG 2003.11.21		Photographer: David Wang
	SCAN0005.JPG、BY003 PSC 013UM 256M DDR2M.BMP	Nov. 21st, 2003	Photographer: David Wang

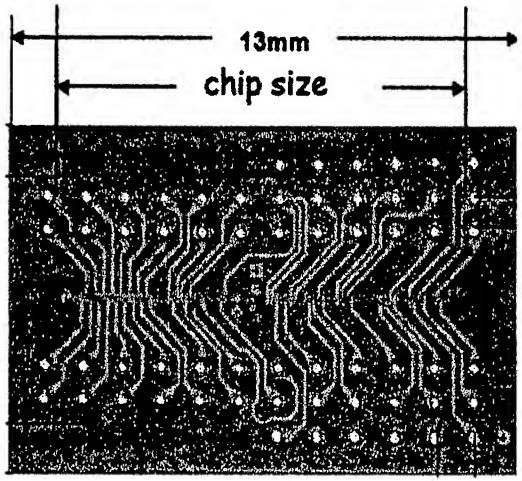
FO WLP for DDR 0.8mmx1.0mm pitch



FO-WLP – Project development layout drawing / photo

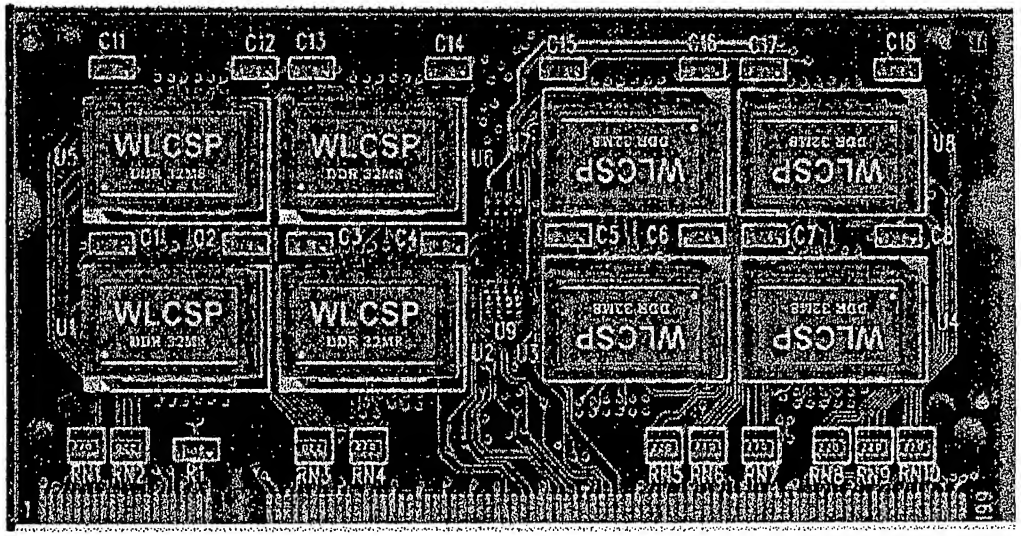
RDL Layout drawing





FO-WLP package view

SO-DIMM w/FO-WLP



Affidavit of Facts

I, David Wang (王誌榮) , was a RDII Leader of ACE (Advanced Chip Engineering Inc.) formerly, a company organized under the laws of Taiwan, R.O.C., and having a business address of No.65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu, Taiwan, R.O.C.

I hereby attest that, on November 21, 2003, I took two pictures of WLP package and memory module. It was my responsibility to develop and test the products in the pictures.

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature David Wang

Date Sep 11. 2006

Doc No	File (File Date)	Date	Testimony of Custodian or Qualified Witness
9-1	921121.JPG	Nov. 21st, 2003	News Paper: Commercial Times
9-2	PRODUCT.DOC 2003.11.21		File Author: Eddy Mo

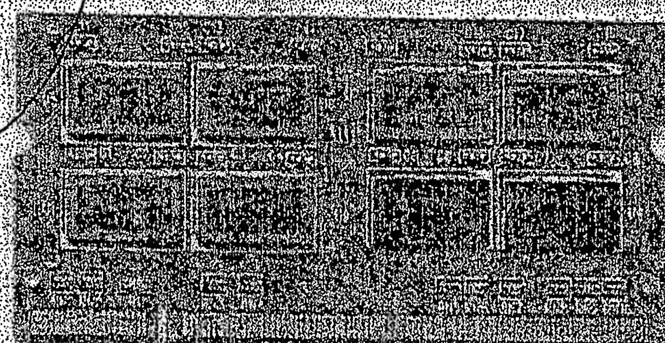
9 - 1

FO-WLP – News announcement

Nov. 21th, 2003

科技專輯　中華民國九十二年十一月二十一日　星期五　24

裕沛WLCSP量產



【記者王瑞發／新竹報導】成立於二000年的裕沛科技積極研發投入，於今年三月開發完成與入量產二五六Mb DDR晶片CSP（見圖，裕沛公司提供）封裝產品，提供客戶尚需保、晶粒大小封裝（chip size）的高階產品，現使用於筆記型電腦與迷你電腦等領域，晶圓級封裝良率達到百分之九十九以上，而該公司由於進行體質調整，預計今年底將辦理現金增資，對裕沛未來發展將有極大助益，預估明年全年營收也將有八億元水準。

裕沛科技董事長楊文焜表示，該公司在發展藍圖規劃方向上，朝市場導向，依據市場趨勢，建構成專業的整合性IC測試封裝研發製造公司，提供完備的晶圓測試、封裝等服務項目。裕沛科技不斷研發新技術以提高的封裝測試技術服務，支援客戶獲得極佳的產品性能，現今已開發完成改良型晶圓級封裝技術，可應用於任何尺寸晶片（含110nm晶片）且產品封裝後可以完全與JEDEC標準相容，更可以依客戶的需求提供可調整的外觀尺寸大小與厚度。裕沛科技已經於十一月份開始使用新技術量產110nm DDR晶片提供客戶高頻與高容量產品，另外，知名DRAM大廠亦與裕沛合作進行驗證JEDEC標準相容（FBGA）之產品，隨時可提供低成本高效能之封裝測試技術予合作廠商。

楊文焜指出，裕沛科技WL-CSP的封裝良率達百分之九十八以上，而且量產模組100000片以上，其WL-CSP模組組裝良率達百分之九十六以上，裕沛科技目前已接到知名大廠客戶的訂單，並提昇公司生產規模與效益以創造更高利潤。裕沛科技現在已經順利開發出全世界第一套WL-CSP記憶體模組，其記憶容量與高頻之產品特性均非其它同業公司所能做到，此項產品已經在市場上獲得客戶極高的評論。

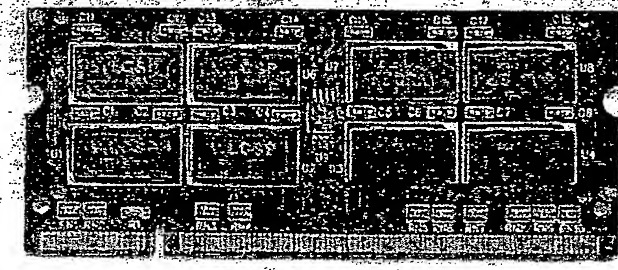
裕沛是台灣第一家投入自行創新研發晶圓級封裝(WLCSP)、晶圓級預燒(WLBI)、晶圓級成品測試(WLFT)、晶圓級基板組裝(WLBA)等技術，與世界晶圓級IC後段技術趨勢同步，並已取得美國三項重要專利，台灣十一項專利，更擁有堅強的研發與技術團隊。

9.

裕沛WLCSP與世界封裝技術同步

【記者王清發／新竹報導】成立於二〇〇〇年的裕沛科技歷經三年研發投入，於今年三月開發完成導入量產二五六Mb DDR WL-CSP（見圖，裕沛公司提供）封裝產品，提供客戶高頻率、晶粒大小封裝（chip size）的高階產品，可使用於筆記型電腦與超頻電腦等領域，晶圓級封裝良率達到百分之九十九以上，而該公司由於進行除資調整，預計今年底將辦理減資再增資，對裕沛未來營運發展將有極大助益，預估明年全年營收也將有八億元水準。

裕沛科技董事長楊文焜表示，該公司在發展藍圖規劃方在市場導向，依據市場趨勢，建構成專業的整合性IC測試封裝研發製造公司，提供完備的晶圓測試、封裝等服務項目，裕沛科技不斷研發新技術以優良的封裝測試技術與服務，支援客戶獲得極佳的產品性能，現今已開發完成改良型晶圓級封裝技術，可應用於任何尺寸晶片（含三〇〇mm晶片）且產品封裝後可以完全與JEDEC標準相容，更可以依客戶的需求提供可調整的外觀尺寸大小與厚度。裕沛科技已擬於十一月份開始使用新技術量產二五六Mb DDR晶片提供客戶高頻與高容量產品，另外，知名DRAM大廠亦與裕沛合作進行驗證JEDEC標準相容（FBGA）之產品，屆時可提供低成本高效能之封裝測試技術予合作廠商。



楊文焜指出，裕沛科技WL-CSP的封裝量產良率達百分之九十八以上，而且量產模組三〇〇〇〇片以上，其WL-CSP模組組裝量產良率達百分之九十六以上。裕沛科技目前已接到知名大廠客戶的訂單，並提昇公司生產規模與效益，以創造更高利潤。裕沛科技現在已經順利開發出全世界第一套WL-CSP記憶體模組，其記憶容量與高頻之產品特性均非其它同業公司所能做到，此項產品已經在市場上獲得客戶極高的評論。

裕沛是台灣第一家國人自行創新研發晶圓級封裝（WLCSP）、晶圓級預燒（WLBI）、晶圓級成品測試（WLFT）、晶圓級基板組裝（WLBA）等技術，與世界晶圓級IC後段技術趨勢同步，並已取得美國三項重要專利、台灣十一項專利，更擁有堅強的研發製造團隊。

建準榮獲工業永續精銳獎

【記者周榮發／高雄報導】甫於今年九月份榮獲經濟部產業科技發展獎的建準電機，近日再傳捷報，榮獲中華民國製造業最高榮譽獎項「二〇〇三年工業永續精銳獎」殊榮，將於二十日於經濟部公務人力會館舉辦頒獎典禮。

該公司董事長洪銀樹表示，建準電機產品為微型散熱風扇和各式精密馬達，並自創品牌SUNON行銷全球，目前已是全球精密散熱處理方案的領導品牌；此次得獎，除企業的經營努力受到多方肯定，更可以重新檢視企業的不足及待改善，是進行企業內部大幅發展的最佳時機，因此企業內部的自我競賽是參賽的最大收穫。

洪銀樹指出，公司係以研發為主軸，多年來已陸續榮獲產業科技發展獎、國家發明獎、國家產品形象獎、東元科技獎等代表性大獎，產品不斷的推陳出新，為因應世界環保潮流，領先業界推出環保型塑風扇、環保鼓風扇以及Maglev磁浮馬達風扇等產品，由於低耗能、無污染、精簡成本且兼顧最佳運作效率，遂獲得世界知名電腦及電子設備大廠的指定使用，全球筆記型電腦所採用的微型散熱風扇，有將近五成採用SUNON的產品，而伺服器、投影機等高階散熱需求的產品，也佔有相當大的比例，足可證明SUNON在散熱領域之專業能力。

洪銀樹強調，為了加強綠色設計及推廣重視環保的決心，所生產的每一件產品，不僅無公害、無污染，且材料規格要求皆符合ISO一四〇〇一及全球先進國家各大廠環保規範標準，產品所採用的原物料、零組件，到包裝材質均為環保可回收材料；如廣受好評的Green Motor系列產品、Maglev磁浮馬達風扇、毫米科技風扇等眾多環保概念產品，均是在Environmentally Caring的綠色環境理念下開發出來的，亦是建準得以在全球精密微型馬達風扇產業中，市場佔有率領先的原因。

9 - 2

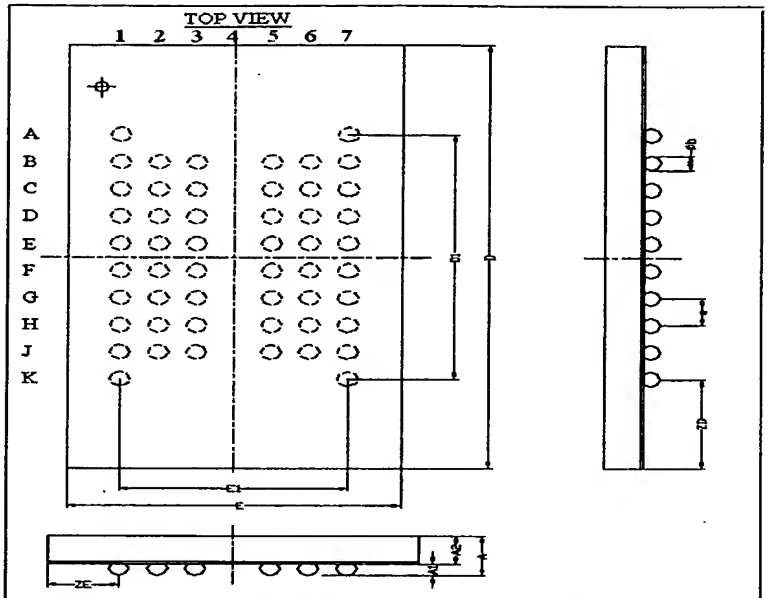
DRAM Product List

256M DDR CSP

Speed Grade	Clock Rate CL=2.5	Data Rate CL=2.5	VDD	VDDQ
-40	250MHz	500MBps	2.6±0.1v	2.6±0.1v
-43	233MHz	466MBps	2.6±0.1v	2.6±0.1v
-46	217MHz	433MBps	2.6±0.1v	2.6±0.1v
-50	200MHz	400MBps	2.6±0.1v	2.6±0.1v
-60	166MHz	333MBps	2.5±0.2v	2.5±0.2v

256Mb Product Configuration List

1. 32MX8 CSP



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOR	MAX	MIN	NOR	MAX
A		0.925				
A1		0.400				
A2	0.500	0.525	0.550			
ϕb		0.450				
D	11.603	11.644	11.685			
D1		6.750				
E	6.511	6.552	6.593			
E1		4.500				
e		0.750				
ZD		2.468				
ZE		1.047				

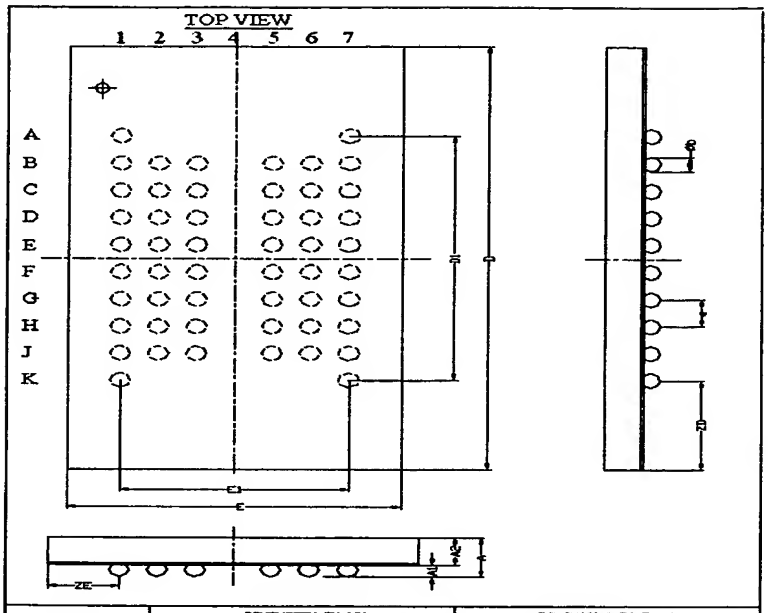
PIN ASSIGNMENT (Top View) –52 balls 0.75um Pitch CSP

	1	2	3	4	5	6	7
A	NC	-	-	-	-	-	NC
B	Vdd	DQ0	VddQ	-	VssQ	DQ7	Vss
C	Vdd	DQ1	DQ2	-	DQ5	DQ6	Vss
D	VddQ	DQ3	VddQ	-	VssQ	DQ4	VssQ
E	/CAS	Vref	Vdd	-	Vss	DQM	DQS
F	A12	/RAS	/WE	-	/CLK	CLK	NC
G	A1	BA1	CKE	-	/CS	A9	A6
H	A3	A10	BA0	-	A11	A8	A4
J	Vdd	A2	A0	-	A7	A5	Vss
K	NC	-	-	-	-	-	NC

Target Product : 256M/512M DIMM DDR 400/433/466/500

512M SODIMM DDR 333/400/433/466/500

2. 64MX4 CSP



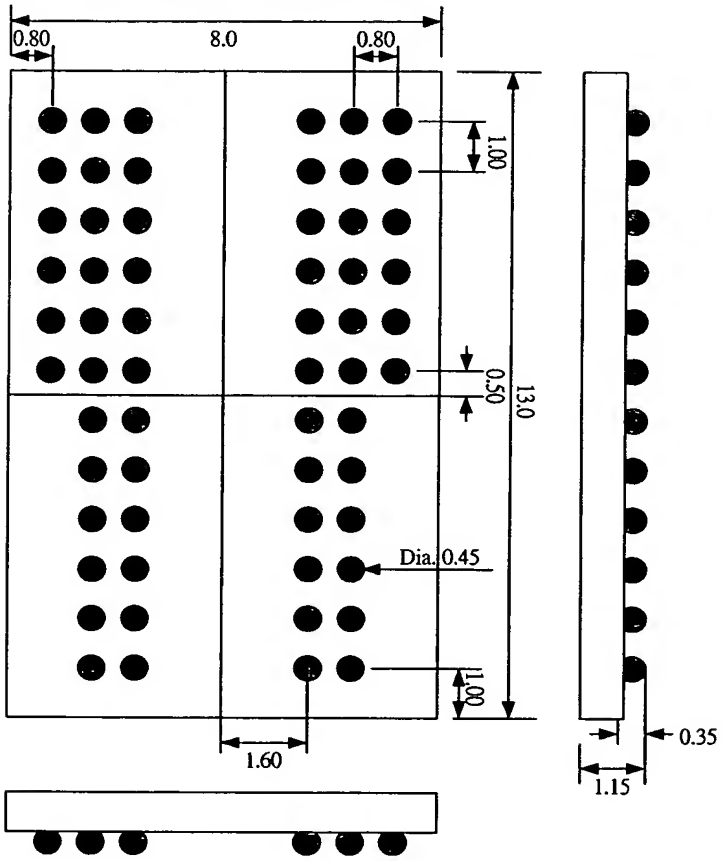
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOR	MAX	MIN	NOR	MAX
A		0.925				
A1		0.400				
A2	0.500	0.525	0.550			
ϕb		0.450				
D	11.603	11.644	11.685			
D1		6.750				
E	6.511	6.552	6.593			
E1		4.500				
e		0.750				
ZD		2.468				
ZE		1.047				

PIN ASSIGNMENT (Top View) –52 balls 0.75um Pitch CSP

	1	2	3	4	5	6	7
A	NC	-	-	-	-	-	NC
B	Vdd	NC	VddQ	-	VssQ	NC	Vss
C	Vdd	DQ0	NC	-	NC	DQ3	Vss
D	VddQ	DQ1	VddQ	-	VssQ	DQ2	VssQ
E	/CAS	Vref	Vdd	-	Vss	DQM	DQS
F	A12	/RAS	/WE	-	/CLK	CLK	NC
G	A1	BA1	CKE	-	/CS	A9	A6
H	A3	A10	BA0	-	A11	A8	A4
J	Vdd	A2	A0	-	A7	A5	Vss
K	NC	-	-	-	-	-	NC

Target Product : 1GB DIMM DDR 400/433/466/500

3. 64MX4 JEDEC Standard CSP

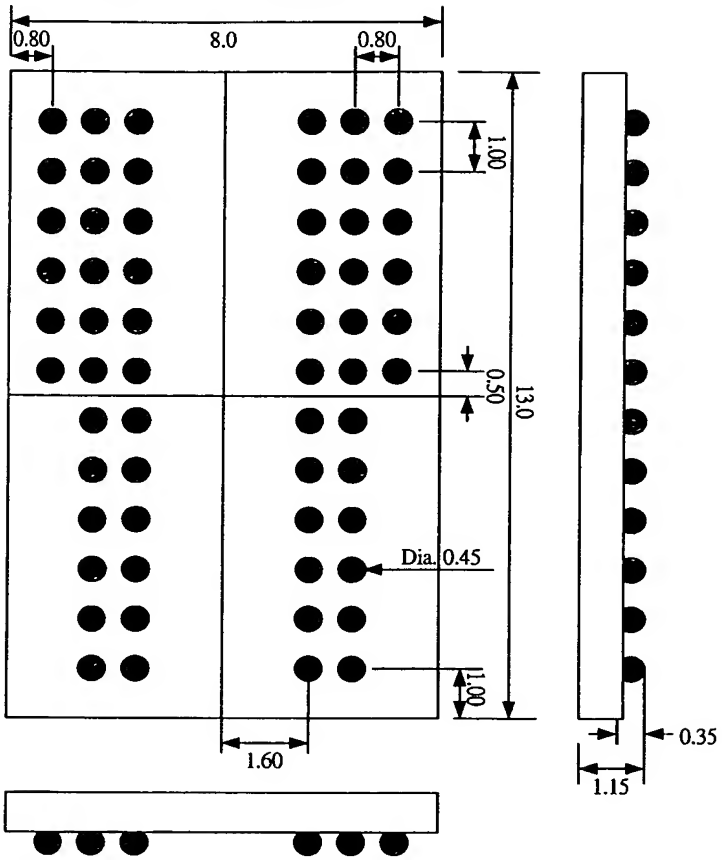


X4

1	2	3		7	8	9
VSSQ	NC	VSS	A	VCC	NC	VCCQ
NC	VCCQ	DQ3	B	DQ0	VSSQ	NC
NC	VSSQ	NC	C	NC	VCCQ	NC
NC	VCCQ	DQ2	D	DQ1	VSSQ	NC
NC	VSSQ	DQS	E	NC	VCCQ	NC
Vref	VSS	DQM	F	NC	VCC	NC
	CLK	/CLK	G	/WE	/CAS	
	A12	CKE	H	/RAS	/CS	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VCC	A3	

Target Product : 1GB DIMM DDR 400/433/466/500

4. 32MX8 JEDEC Standard CSP



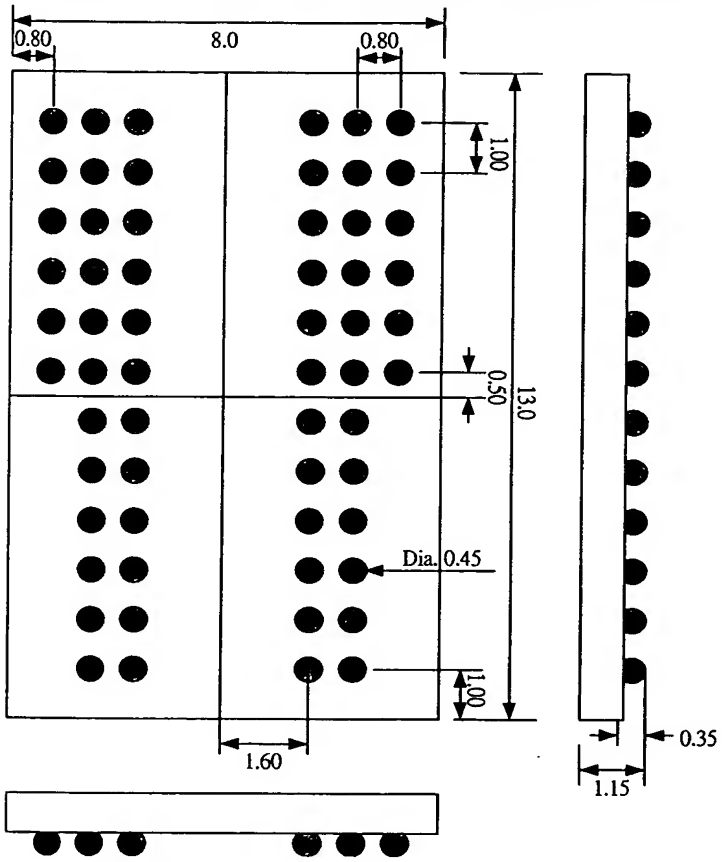
PIN ASSIGNMENT (Top View)

X8

1	2	3		7	8	9
VSSQ	DQ7	VSS	A	VCC	DQ0	VCCQ
NC	VCCQ	DQ6	B	DQ1	VSSQ	NC
NC	VSSQ	DQ5	C	DQ2	VCCQ	NC
NC	VCCQ	DQ4	D	DQ3	VSSQ	NC
NC	VSSQ	DQS	E	NC	VCCQ	NC
Vref	VSS	DQM	F	NC	VCC	NC
	CLK	/CLK	G	/WE	/CAS	
	A12	CKE	H	/RAS	/CS	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VCC	A3	

Target Product : 256M/512M DIMM DDR 400/433/466/500 for OEM customer

5. 16MX16 (32MX8 Ball assignment option) JEDEC Standard CSP



PIN ASSIGNMENT (Top View)

X16

1	2	3		7	8	9
VSSQ	DQ15	VSS	A	VCC	DQ0	VCCQ
DQ14	VCCQ	DQ13	B	DQ2	VSSQ	DQ1
DQ12	VSSQ	DQ11	C	DQ4	VCCQ	DQ3
DQ10	VCCQ	DQ9	D	DQ6	VSSQ	DQ5
DQ8	VSSQ	UDQS	E	LDQS	VCCQ	DQ7
Vref	VSS	UDQM	F	LDQM	VCC	Option
	CLK	/CLK	G	/WE	/CAS	
	A12	CKE	H	/RAS	/CS	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VCC	A3	

Target Product : Graphic Application

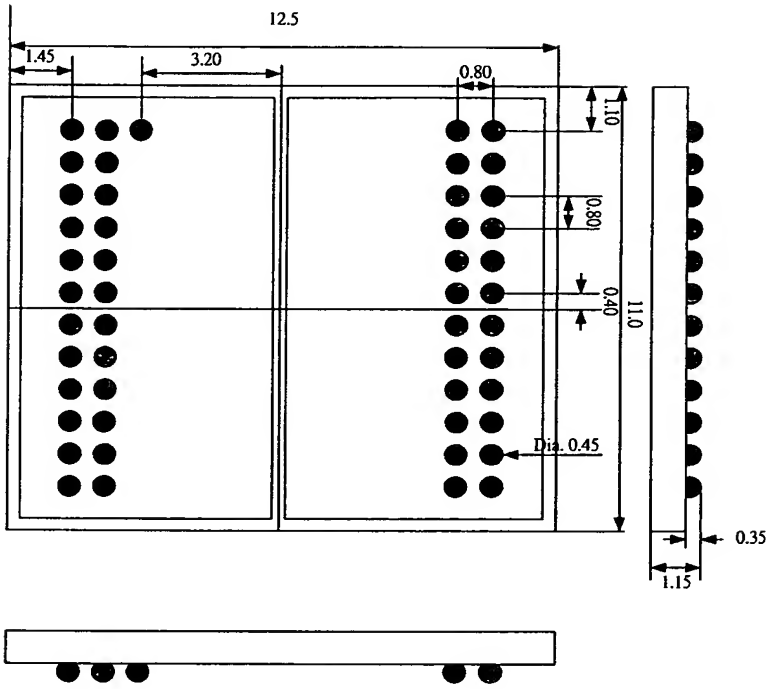
512Mb DDR CSP

Speed Grade	Clock Rate CL=2.5	Data Rate CL=2.5	VDD	VDDQ
-46	217MHz	433MBps	2.6±0.1v	2.6±0.1v
-50	200MHz	400MBps	2.6±0.1v	2.6±0.1v
-60	166MHz	333MBps	2.5±0.2v	2.5±0.2v

Target Product : 1GB SODIMM DDR 333/400/433/466/500

1. 64MX8 (2 Chips combo)

(Available in December 2003)



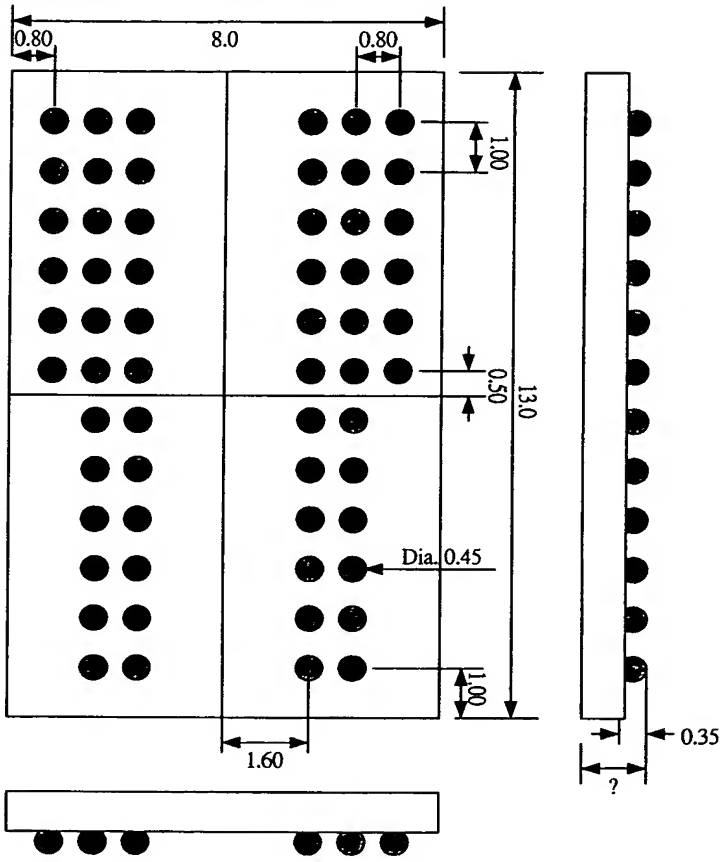
PIN ASSIGNMENT (Top View)

1	2	3	X8	11	12	13
VSSQ	DQ7	VSS	A		DQ0	VCCQ
VCCQ	DQ6		B		DQ1	VSSQ
VSSQ	DQ5		C		DQ2	VCCQ
VCCQ	DQ4		D		DQ3	VSSQ
VSSQ	DQS		E		NC	VCCQ
VSS	DQM		F		Vref	VCC
CLK	/CLK		G		/WE	/CAS
A12	CKE		H		/RAS	/CS
A11	A9		J		BA1	BA0
A8	A7		K		A0	A10/AP
A6	A5		L		A2	A1
A4	VSS		M		VCC	A3

X16

1	2	3		13	14	15
VSSQ	DQ15	VSS	A	VCC	DQ0	VCCQ
DQ14	VCCQ	DQ13	B	DQ2	VSSQ	DQ1
DQ12	VSSQ	DQ11	C	DQ4	VCCQ	DQ3
DQ10	VCCQ	DQ9	D	DQ6	VSSQ	DQ5
DQ8	VSSQ	UDQS	E	LDQS	VCCQ	DQ7
Vref	VSS	UDQM	F	LDQM	VCC	Option
	CLK	/CLK	G	/WE	/CAS	
	A12	CKE	H	/RAS	/CS	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VCC	A3	

2. 64MX8 (2 Chips Stack) JEDEC Standard CSP
(Available in January 2004)

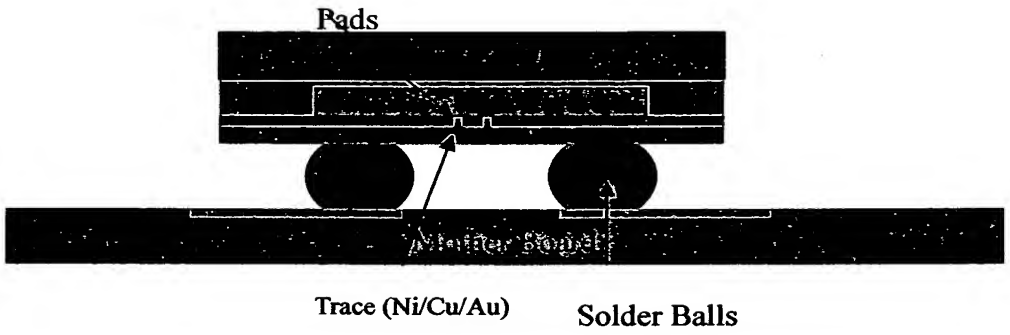


PIN ASSIGNMENT (Top View)

X8

1	2	3		7	8	9
VSSQ	DQ7	VSS	A	VCC	DQ0	VCCQ
NC	VCCQ	DQ6	B	DQ1	VSSQ	NC
NC	VSSQ	DQ5	C	DQ2	VCCQ	NC
NC	VCCQ	DQ4	D	DQ3	VSSQ	NC
NC	VSSQ	DQS	E	NC	VCCQ	NC
Vref	VSS	DQM	F	NC	VCC	NC
	CLK	/CLK	G	/WE	/CAS	
	A12	CKE	H	/RAS	/CS	
	A11	A9	J	BA1	BA0	
	A8	A7	K	A0	A10/AP	
	A6	A5	L	A2	A1	
	A4	VSS	M	VCC	A3	

WLCSP cross section structure



育霈科技股份有限公司
Advanced Chip Engineering Technology Inc.

離職證明書
Resignation Certification

姓　名 Name	牟慶聰 Eddy Mou	出生日期 Date of Birth	民國51年09月20日 20-Sep-62
身份證字號 I.D. No	L121816080	性　別 Sex	男 Male
服務部門 Department	總經理室 President Office	職　稱 Job Title	副總經理 Vice President
到職日 Date of Employment	民國89年05月01日 01-May-00	離職日 Date of Leaving	民國93年09月30日 30-Sep-04
備　註 Remark	空白 Nil		

上述各項屬實，特此證明。
This is to certify that the above statements are true and correct.

人力資源部
Human Resources Department

育霈科技股份有限公司 人事專用章 新竹縣湖口鄉光復北路65號

中華民國九十五年八月十一日
Date：August 11, 2006

地址：新竹縣303新竹工業區光復北路六十五號　電話:03-5983232
Add： No.26, Kuang-Fu North Rd., Hsin-Chu Industrial Park, Hsin-Chu 303, Taiwan, R.O.C.
TEL：886-03-5983232　FAX：886-5986565

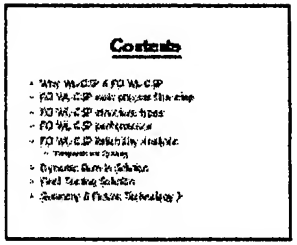
Doc No	File (File Date)	Date	Testimony of Custodian or Qualified Witness
10-1	ENHANCED WLCSP_APIA.PDF Wafer Level Technology_ACET.ppt	Dec. 4th, 2003	File Author: Wen-kun Yang
10-2	IC Packaging.ppt 2004.3.14		File Author: Wen-kun Yang
10-3	YIELD ANALYSIS OF LOT_61_63.DOC 2004.3.31	Mar. 31st, 2004	Analyst: David Wang

10 - 1

Dec. 4th, 2003

FO-WLP – Presented in SEMI-JAPAN

1



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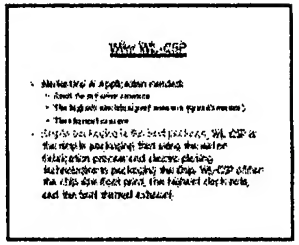
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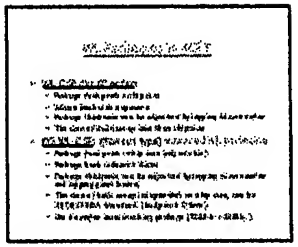
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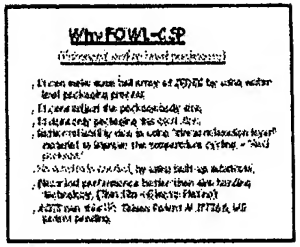

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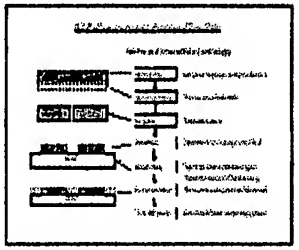
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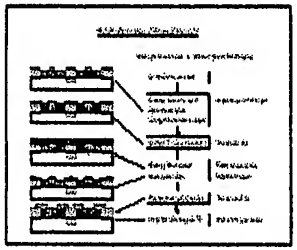
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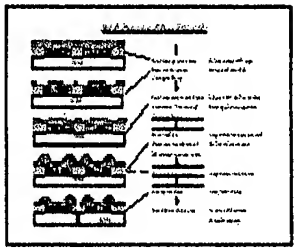
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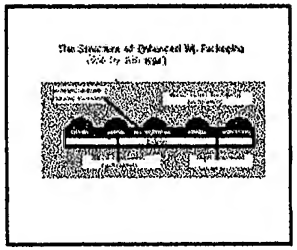
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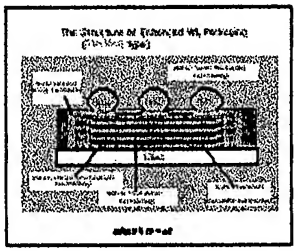
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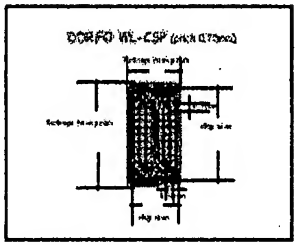
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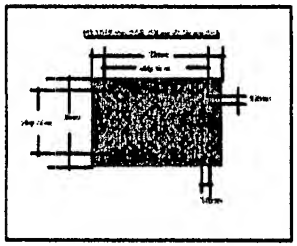
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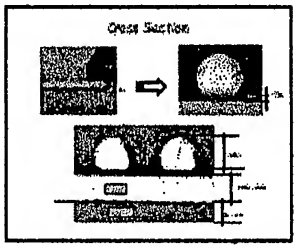

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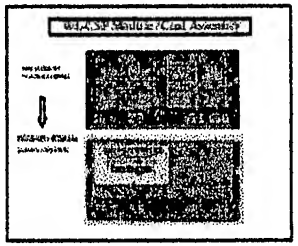
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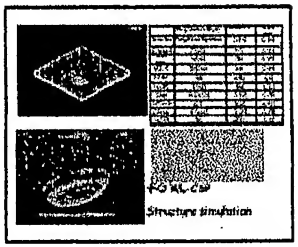

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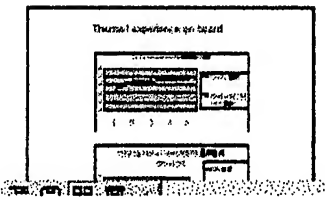
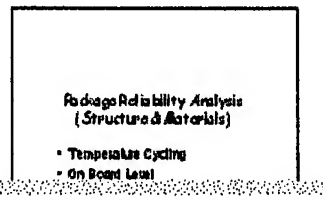
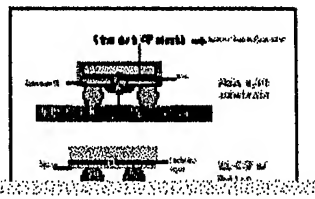
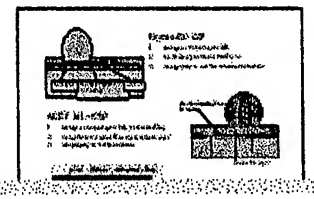
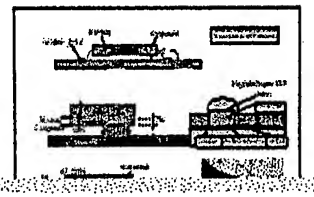








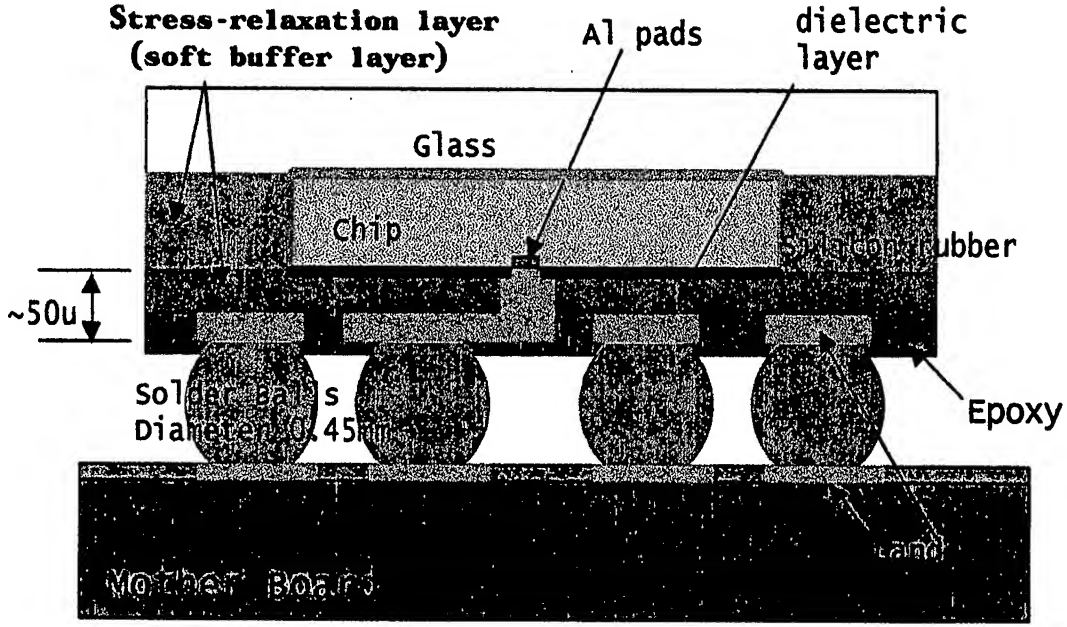


ACET enhanced WLP

1. Using electro plating for RDL (thickness >15u)
2. Using Dielectric layer/PI/silicon rubber as stress release layer
3. Using epoxy to hold solder balls
4. Better thermal conductivity (Glass)

Due to WLP is making the built up substrate on the top of circuit side, the property of 3170 (thick layer) and silicon rubber can absorb the CTE mismatching during the temperature cycling, the metal and epoxy layers can follow up the extension of FR4 materials, actual it is similar with FR4, but 3170 absorb most stress.

ACET FO WLP



Dielectric Layer

1. Siloxane content: Medium
2. Elastic film: 25 ~30u
3. Low young's modulus: 90 MPa
4. Adhesion strength: >500hrs
5. Moisture uptake: <0.2%

WKYang6699(楊文焜)

寄件者: Galen Fong [gfong@ultratech.com]
寄件日期: 2006年8月15日星期二 上午 8:45
收件者: WKYang6699(楊文焜)
主旨: RE: Message from WK Yang (ACET)

附件: ACETechnology.pdf

ACETechnology.pdf (497 KB)

Hello WK,

Attached is your presentation from the 2003 APiA Semiar at Semicon Japan. Is this what you are looking for?

Regards,
Galen

>>> WKYang6699(***) <wkyang@ace-tek.com.tw> 8/13/2006 5:52 PM >>>
Dear Galen,
Thank you for your kindly help.

Best regards,
WK Yang

-----Original Message-----
From: Galen Fong [mailto:gfong@ultratech.com]
Sent: Sunday, August 13, 2006 4:07 AM
To: WKYang6699(***)
Cc: Scott Zafiropoulo
Subject: Re: Message from WK Yang (ACET)

Hello WK.

Good to hear from you! I am doing fine. Things are going well at Ultratech. How are you?

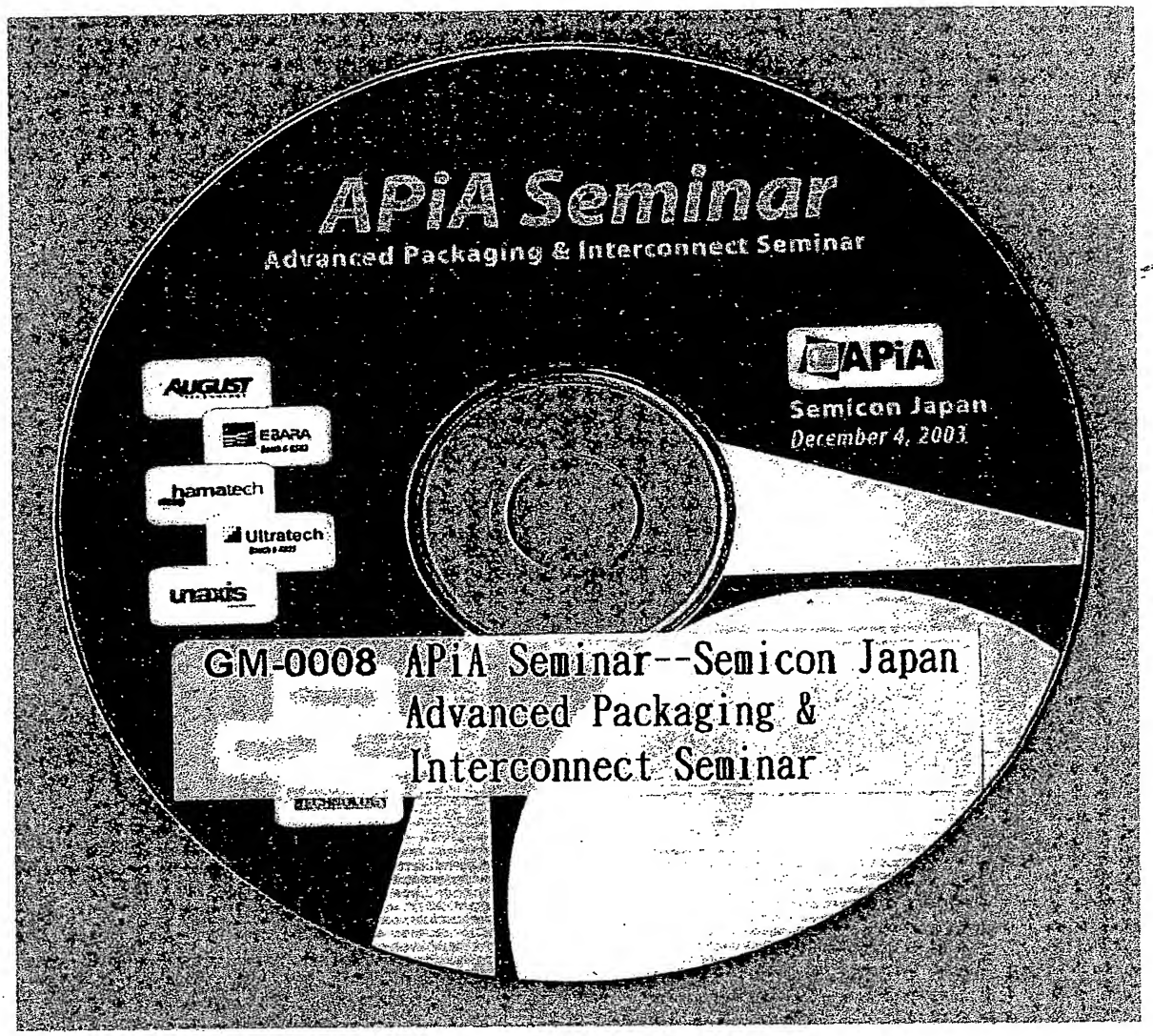
I will ask our Marketing Communication to look up the presentation and send you a copy.

Best regards,
Galen

>>> WKYang6699($(G·*¤åµO) <wkyang@ace-tek.com.tw> 8/7/2006 10:37 PM >>>
Hello Galen, This is WK Yang from ACET in Taiwan Long time no see, How are you!
Recently, I am collecting the document that I have created and attend the meeting before. Did you remember that you invited me to attend the APiA seminar in Japan on Dec. 2003. Since I can not find the document (CD) that APiA publish it and offer this materials to who attend the meeting, so, Do you still have the copy of seminar presentation of APiA (CD) or electrical file that I present it during the seminar. If you still have this materials, may I ask you to send one copy to me?

Thank you for your help and supporting.

Best regards,
WK Yang
Advanced Chip Engineering Technology,
email: wkyang@ace-tek.com.tw
phone: 886-3-5983232 x 6699

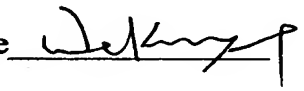

APiA Seminar
Advanced Packaging & Interconnect Seminar
APiA
Semicon Japan
December 4, 2003
AUGUST
EBARA
hamatech
Ultratech
unaxis
GM-0008 APiA Seminar--Semicon Japan
Advanced Packaging &
Interconnect Seminar

Affidavit of Facts

I, Wen-kun Yang (楊文焜), am a C.E.O of ACE (Advanced Chip Engineering Technology Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No. 65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu 303, Taiwan, R.O.C.

I hereby attest that, on December 4, 2003, I have been invited to offer the presentation in Semi Japan by Advanced Packaging interconnect associate (APIA), at that time, I have presented the enhanced WLCSP (Fan-out type WLP) during the presentation。

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature 

Date Sept. 11, 2006

10 - 2

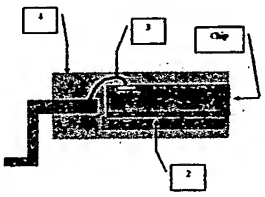
IC Packaging Analysis

Structure & Performance

Advanced Chip Engineering Technology Inc.

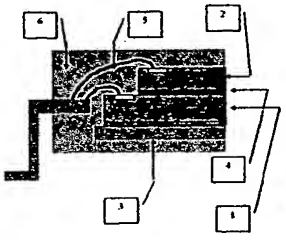
For Internal Use Only

TSOP/QFP



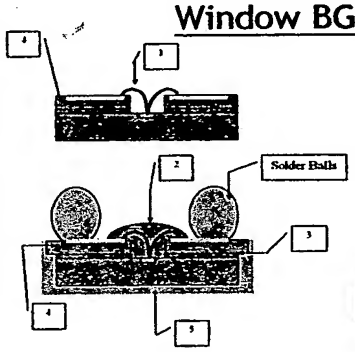
Key items:
1. Standard packaging
2. Lead frame based
3. Low profile wire bonding tech.
4. Molding flow pressure
5. Lead on chip lead frame for center pads

Multi Chip Package



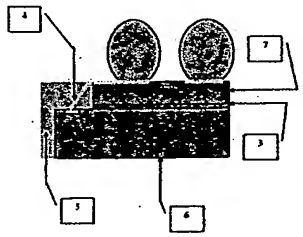
Key items:
1. Chip stress during wire bonding
2. KGD issue
3. Lead frame based
4. Buffer materials and process between two chip
5. Low profile wire bonding tech.
6. Molding flow pressure
7. No use for center pads

Window BGA



Key items:
1. Low profile wire bonding
2. Use the liquid resin or mold resin
3. Buffer materials and process between substrate and chip
4. Substrate based
5. Chip outside molding (optional process)
6. u-BGA pattern issue
7. Higher cost

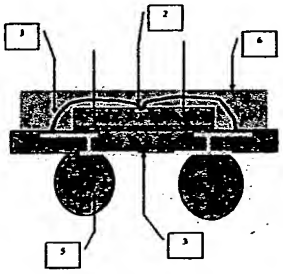
u BGA



Key Items:
1. Pattern issue(Tessera)
2. Process equipment /Production issue
3. Buffer material between substrate and chip
4. Lead bonding process
5. Side wall molding process
6. Silicon exposed issue (back side)
7. Substrate based

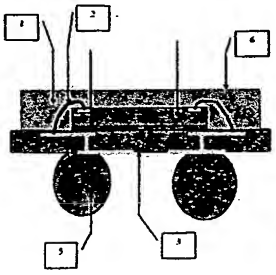
u BGA: Tessera IP

Tiny BGA, Mini BGA, FBGA (I)



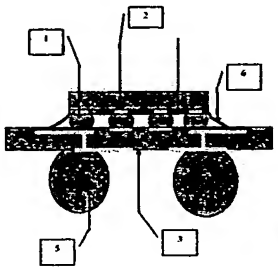
Key items:
1. Standard BGA process
2. Longer wire process for central pads, high lead inductance
3. Substrate based
4. Large package size
5. Ball pitch @ 0.75mm or 0.8mm
6. Molding process

Tiny BGA, Mini BGA, FBGA (II)



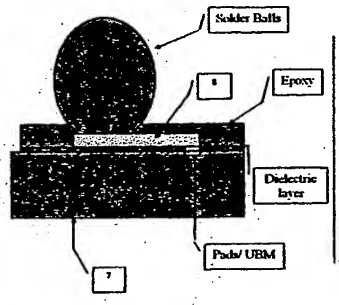
Key items:
1. Standard BGA process
2. wire bonding process for bonding pads, high lead inductance
3. Substrate based
4. Large package size
5. Ball pitch @ 0.75mm or 0.8mm
6. Molding process

Flip Chip BGA / FCIP



Key items:
1. Solder bumping process (wafer level process)
2. Chip
3. Substrate based
4. Large package size
5. Ball pitch > 1.2mm
6. Under fill process

WL-CSP

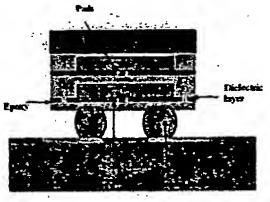


Key items:
1. Wafer level process
2. Use photo mask
3. No lead inductance
4. No substrate
5. No wire bonding
6. No molding
7. No back side molding (Silicon Exposed)
8. Re-distribution by plating (Cu/Ni/Au)
9. Pads location in-depends

FO WL-CSP

Key items:
1. Wafer level process
2. Use photo mask
3. No lead inductance
4. No substrate
5. No wire bonding
6. No molding
7. Back side with Glass
8. Re-distribution by plating (Cu/Ni/Au)
9. Pads location in-depends
10. Package size > chip size

WL-CSP (stacking)



Key items:
1. Wafer level process
2. Use photo mask
3. No lead inductance
4. No substrate
5. No wire bonding
6. No molding
7. back side bonding w/Glass
8. Re-distribution by plating (Cu/Ni/Au)
9. Pads location in-depends

Affidavit of Facts

I, Wen-kun Yang (楊文焜), am a C.E.O of ACE (Advanced Chip Engineering Technology Inc.), a company organized under the laws of Taiwan, R.O.C., and having a business address of No. 65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu 303, Taiwan, R.O.C.

I hereby attest that, on March 14th 2004, I have created the presentation file of IC Packaging that present the several types of IC packaging including the fan-in and fan-out type etc. It be used for internal discussion。

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

Signature 

Date Sept. 11, 2006

10 - 3

Yield Analysis of Lo# 61 & 63 Date 3/31/04

LOT NO :E04030061 WaferId :01
TESTER NO :T8201 P/C NO :-7 OPER.NO :A277

BIN	COUNT	YIELD %
UNITS TESTED	348	
UNITS PASS	143	41 %
BIN 1 PASS-400 CL=2.5	69	19 %
BIN 3 PASS-400 CL=2.0	74	21 %
BIN 5 GROSSFUNCTION FAIL	18	5 %
BIN 6 REFRESH FAIL	2	0 %
BIN 6 SPEED FAIL	16	4 %
BIN 7 LEAKAGE FAIL	7	2 %
BIN 8 CONTINU FAIL	162	46 %

Station 1 Summary Report Finished !!

LOT NO :E04030061 WaferId :02
TESTER NO :T8209 P/C NO :-2 OPER.NO :A277
##

BIN	COUNT	YIELD %
UNITS TESTED	348	
UNITS PASS	324	93 %
BIN 1 PASS-400 CL=2.5	93	26 %
BIN 3 PASS-400 CL=2.0	231	66 %
BIN 5 GROSSFUNCTION FAIL	9	2 %
BIN 6 REFRESH FAIL	1	0 %
BIN 6 SPEED FAIL	2	0 %
BIN 7 LEAKAGE FAIL	7	2 %
BIN 8 CONTINU FAIL	5	1 %

Station 1 Summary Report Finished !!

LOT NO :E04030061 WaferId :03
TESTER NO :T8203 P/C NO :-1 OPER.NO :A277
##

BIN	COUNT	YIELD %
UNITS TESTED	348	
UNITS PASS	311	89 %
BIN 1 PASS-400 CL=2.5	88	25 %
BIN 3 PASS-400 CL=2.0	223	64 %
BIN 5 GROSSFUNCTION FAIL	18	5 %
BIN 6 REFRESH FAIL	3	0 %
BIN 6 SPEED FAIL	0	0 %
BIN 7 LEAKAGE FAIL	5	1 %
BIN 8 CONTINU FAIL	11	3 %

Station 1 Summary Report Finished !!

LOT NO :E04030061 WaferId :04
TESTER NO :T8201 P/C NO :-7 OPER.NO :A277
##

BIN	COUNT	YIELD %
UNITS TESTED	348	
UNITS PASS	308	88 %
BIN 1 PASS-400 CL=2.5	99	28 %
BIN 3 PASS-400 CL=2.0	209	60 %
BIN 5 GROSSFUNCTION FAIL	23	6 %
BIN 6 REFRESH FAIL	3	0 %
BIN 6 SPEED FAIL	3	0 %
BIN 7 LEAKAGE FAIL	2	0 %
BIN 8 CONTINU FAIL	9	2 %

Station 1 Summary Report Finished !!

LOT NO :E04030061 WaferId :05
TESTER NO :T8203 P/C NO :-1 OPER.NO :A277
##

BIN	COUNT	YIELD %
UNITS TESTED	348	

UNITS PASS 287 82 %
BIN 1 PASS-400 CL=2.5 89 25 %
BIN 3 PASS-400 CL=2.0 198 56 %
BIN 5 GROSSFUNCTION FAIL 31 8 %
BIN 6 REFRESH FAIL 5 1 %
BIN 6 SPEED FAIL 3 0 %
BIN 7 LEAKAGE FAIL 13 3 %
BIN 8 CONTINU FAIL 9 2 %
Station 1 Summary Report Finished !!

LOT NO :E04030063 WaferId :01
TESTER NO :T8209 P/C NO :-2 OPER.NO :A277
##

BIN	COUNT	YIELD %
UNITS TESTED	348	
UNITS PASS	299	85 %
BIN 1 PASS-400 CL=2.5	68	19 %
BIN 3 PASS-400 CL=2.0	231	66 %
BIN 5 GROSSFUNCTION FAIL	17	4 %
BIN 6 REFRESH FAIL	3	0 %
BIN 6 SPEED FAIL	1	0 %
BIN 7 LEAKAGE FAIL	2	0 %
BIN 8 CONTINU FAIL	26	7 %

Station 1 Summary Report Finished !!

LOT NO :E04030063 WaferId :02
TESTER NO :T8203 P/C NO :-1 OPER.NO :A277
##

BIN	COUNT	YIELD %
UNITS TESTED	348	
UNITS PASS	324	93 %
BIN 1 PASS-400 CL=2.5	69	19 %
BIN 3 PASS-400 CL=2.0	255	73 %
BIN 5 GROSSFUNCTION FAIL	2	0 %

BIN 6 REFRESH FAIL 6 1 %

BIN 6 SPEED FAIL 0 0 %

BIN 7 LEAKAGE FAIL 3 0 %

BIN 8 CONTINU FAIL 13 3 %

Station 1 Summary Report Finished !!

LOT NO :E04030063 WaferId :03

TESTER NO :T8203 P/C NO :-1 OPER.NO :A277

##

BIN	COUNT	YIELD %
UNITS TESTED	348	
UNITS PASS	318	91 %
BIN 1 PASS-400 CL=2.5	85	24 %
BIN 3 PASS-400 CL=2.0	233	66 %
BIN 5 GROSSFUNCTION FAIL	19	5 %
BIN 6 REFRESH FAIL	2	0 %
BIN 6 SPEED FAIL	0	0 %
BIN 7 LEAKAGE FAIL	7	2 %
BIN 8 CONTINU FAIL	2	0 %

Station 1 Summary Report Finished !!

LOT NO :E04030063 WaferId :04

TESTER NO :T8209 P/C NO :-6 OPER.NO :A277

##

BIN	COUNT	YIELD %
UNITS TESTED	348	
UNITS PASS	318	91 %
BIN 1 PASS-400 CL=2.5	99	28 %
BIN 3 PASS-400 CL=2.0	219	62 %
BIN 5 GROSSFUNCTION FAIL	12	3 %
BIN 6 REFRESH FAIL	3	0 %
BIN 6 SPEED FAIL	6	1 %
BIN 7 LEAKAGE FAIL	5	1 %
BIN 8 CONTINU FAIL	4	1 %

Station 1 Summary Report Finished !!

LOT NO :E04030063 WaferId :05

TESTER NO :T8209 P/C NO :-2 OPER.NO :A277

##

BIN	COUNT	YIELD %
UNITS TESTED	348	
UNITS PASS	165	47 %
BIN 1 PASS-400 CL=2.5	26	7 %
BIN 3 PASS-400 CL=2.0	139	39 %
BIN 5 GROSSFUNCTION FAIL	3	0 %
BIN 6 REFRESH FAIL	0	0 %
BIN 6 SPEED FAIL	0	0 %
BIN 7 LEAKAGE FAIL	6	1 %
BIN 8 CONTINU FAIL	174	50 %

Station 1 Summary Report Finished !!

Affidavit of Facts

I, David Wang (王誌榮) , was a RDII Leader of ACE (Advanced Chip Engineering Inc.) formerly, a company organized under the laws of Taiwan, R.O.C., and having a business address of No.65, Kuang-Fu North Rd., Hsin-Chu Industrial Park Hu-Kou, Hsin-Chu, Taiwan, R.O.C.

I hereby attest that, I made the yield analysis of lot # 61 & 63 for Fan-out type WLP, on March 31, 2004; I published the yield rate.

I hereby also declare that all statements made herein are based on my personal knowledge and are true and that these statements are made on the basis of the information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under the applicable United States laws and that such willful false statements might jeopardize the validity of the application or any patent issued thereon.

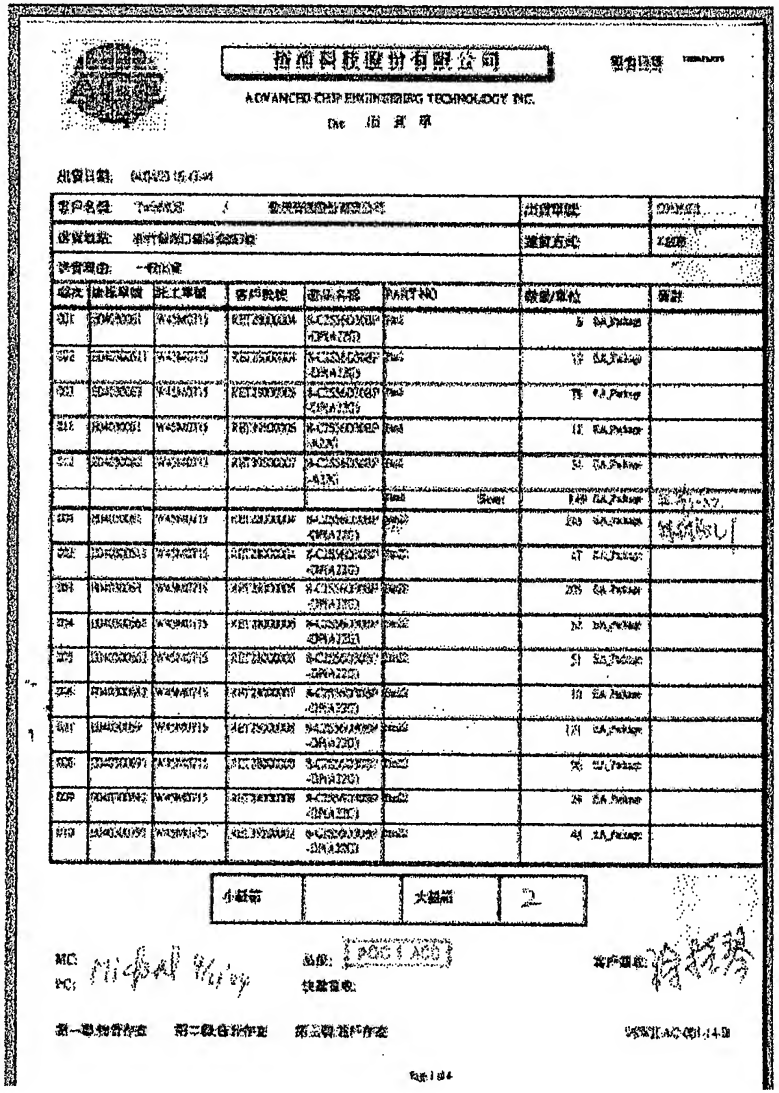
Signature David Wang

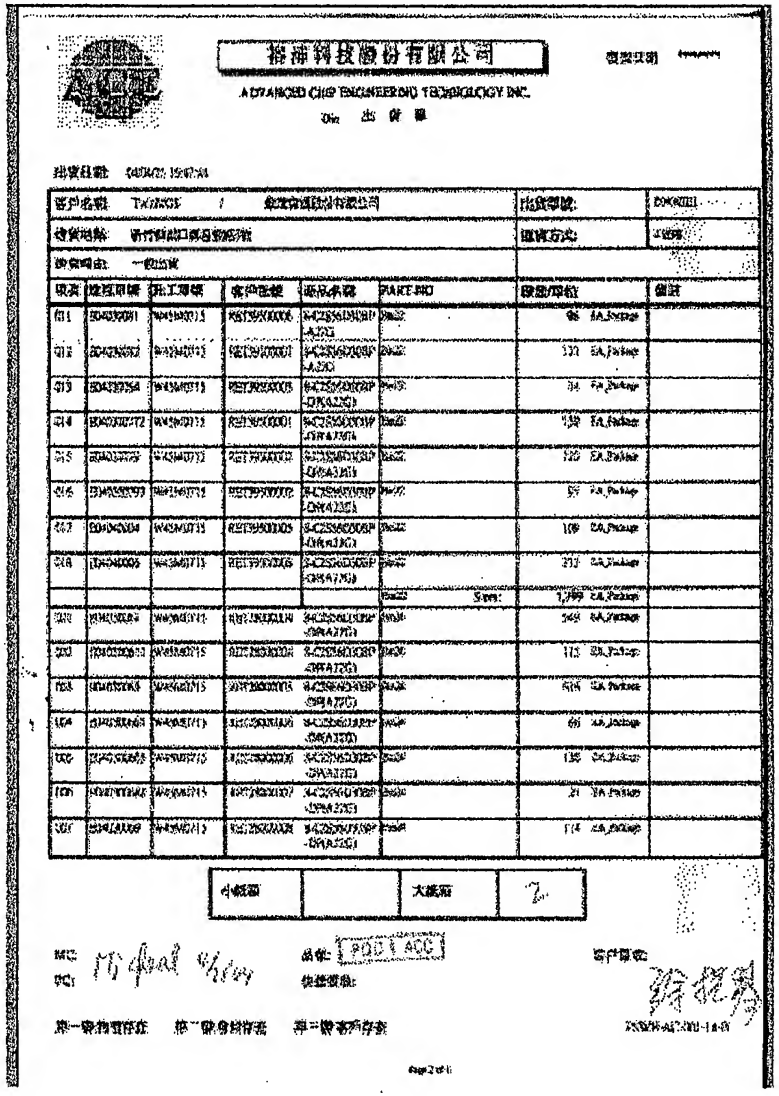
Date Sep 11. 2006

Doc No	File (File Date)	Date	Testimony of Custodian or Qualified Witness
11	TwinMOS出貨單.pdf 2006.6.27	Apr. 21st, 2004	Client: TwinMOS (勤茂資通)

April 21th, 2004

FO-WLP – Volume shipment





裕沛科技股份有限公司

製表日期 2004/4/21

ADVANCED CHIP ENGINEERING TECHNOLOGY INC.

Die 出 貨 單

出貨日期: 04/04/21 16:47:44

客戶名稱:	TwinMOS / 勤茂資通股份有限公司					出貨單號:	D04040011
送貨地點:	新竹縣湖口鄉自強路3號					運貨方式:	2.送達
送貨理由:	一般出貨						
項次	途程單號	託工單號	客戶批號	產品名稱	PART-NO	數量/單位	備註
001	E04030061	W45M0715	RET28000004	8-C2S56D30BP-DP(A22G)	Bin1	6 EA_Package	
002	E040300611	W45M0715	RET28000004	8-C2S56D30BP-DP(A22G)	Bin1	19 EA_Package	
003	E04030063	W45M0715	RET28000005	8-C2S56D30BP-DP(A22G)	Bin1	78 EA_Package	
011	E04030081	W45M0715	RET39500006	8-C2S56D30BP-A22G	Bin1	12 EA_Package	
012	E04030082	W45M0715	RET39500007	8-C2S56D30BP-A22G	Bin1	34 EA_Package	
					Bin1 Sum:	149 EA_Package	正常品
001	E04030061	W45M0715	RET28000004	8-C2S56D30BP-DP(A22G)	Bin22	243 EA_Package	特採1L
002	E040300611	W45M0715	RET28000004	8-C2S56D30BP-DP(A22G)	Bin22	47 EA_Package	
003	E04030063	W45M0715	RET28000005	8-C2S56D30BP-DP(A22G)	Bin22	205 EA_Package	
004	E040300661	W45M0715	RET28000006	8-C2S56D30BP-DP(A22G)	Bin22	52 EA_Package	
005	E040300663	W45M0715	RET28000006	8-C2S56D30BP-DP(A22G)	Bin22	51 EA_Package	
006	E040300682	W45M0715	RET28000007	8-C2S56D30BP-DP(A22G)	Bin22	10 EA_Package	
007	E04030069	W45M0715	RET28000008	8-C2S56D30BP-DP(A22G)	Bin22	121 EA_Package	
008	E040300691	W45M0715	RET28000008	8-C2S56D30BP-DP(A22G)	Bin22	96 EA_Package	
009	E040300692	W45M0715	RET28000008	8-C2S56D30BP-DP(A22G)	Bin22	24 EA_Package	
010	E040300791	W45M0715	RET39500002	8-C2S56D30BP-DP(A22G)	Bin22	48 EA_Package	

小紙箱		大紙箱	2

MC: Michael 4/21'04

PC:

品保: PQC ACC

快遞簽收:

客戶簽收:

第一聯:物管存查 第二聯:會計存查 第三聯:客戶存查

PSWH-AC-001-14-B

裕沛科技股份有限公司

製表日期 2004/4/21

ADVANCED CHIP ENGINEERING TECHNOLOGY INC.

Die 出 貨 單

出貨日期: 04/04/21 16:47:44

客戶名稱:	TwinMOS / 勤茂資通股份有限公司	出貨單號:	D04010011
送貨地點:	新竹縣湖口鄉自強路3號	運貨方式:	2.送達
送貨理由:	一般出貨		

項次	途程單號	託工單號	客戶批號	產品名稱	PART-NO	數量/單位	備註
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012	E04030082	W45M0715	RET39500007	8-C2S56D30BP-A22G	Bin22	121 EA_Package	
013	E04030084	W45M0715	RET39500003	8-C2S56D30BP-DP(A22G)	Bin22	14 EA_Package	
014	E040300772	W45M0715	RET39500001	8-C2S56D30BP-DP(A22G)	Bin22	130 EA_Package	
015	E04030079	W45M0715	RET39500002	8-C2S56D30BP-DP(A22G)	Bin22	120 EA_Package	
016	E040300793	W45M0715	RET39500002	8-C2S56D30BP-DP(A22G)	Bin22	97 EA_Package	
017	E04040004	W45M0715	RET39500005	8-C2S56D30BP-DP(A22G)	Bin22	109 EA_Package	
018	E04040006	W45M0715	RET39500008	8-C2S56D30BP-DP(A22G)	Bin22	215 EA_Package	
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005	E040300663	W45M0715	RET28000006	8-C2S56D30BP-DP(A22G)	Bin24	138 EA_Package	
006	E040300682	W45M0715	RET28000007	8-C2S56D30BP-DP(A22G)	Bin24	21 EA_Package	
007	E04030069	W45M0715	RET28000008	8-C2S56D30BP-DP(A22G)	Bin24	174 EA_Package	

小紙箱		大紙箱	2

MC: Michael 4/21/04

PC:

品保: POC1 ACC

快遞簽收:

客戶簽收:

第一聯:物管存查 第二聯:會計存查 第三聯:客戶存查

PSWH-AC-001-14-B

裕沛科技股份有限公司

製表日期 2004/4/21

ADVANCED CHIP ENGINEERING TECHNOLOGY INC.

Die 出 貨 單

日 日期: 04/04/21 16:47:44

客戶名稱:	TwinMOS / 勤茂資通股份有限公司	出貨單號:	D04040011
送貨地點:	新竹縣湖口鄉自強路3號	運貨方式:	2.送達
送貨理由:	一般出貨		

項次	途程單號	託工單號	客戶批號	產品名稱	PART-NO	數量/單位	備註
008	E040300691	W45M0715	RET28000008	8-C2S56D30BP-DP(A22G)	Bin24	101 EA_Package	特殊BIN3
009	E040300692	W45M0715	RET28000008	8-C2S56D30BP-DP(A22G)	Bin24	7 EA_Package	
010	E040300791	W45M0715	RET39500002	8-C2S56D30BP-DP(A22G)	Bin24	127 EA_Package	
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013	E04030084	W45M0715	RET39500003	8-C2S56D30BP-DP(A22G)	Bin24	21 EA_Package	
014	E040300772	W45M0715	RET39500001	8-C2S56D30BP-DP(A22G)	Bin24	166 EA_Package	
015	E04030079	W45M0715	RET39500002	8-C2S56D30BP-DP(A22G)	Bin24	268 EA_Package	
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003	E04030063	W45M0715	RET28000005	8-C2S56D30BP-DP(A22G)	Bin3	243 EA_Package	
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小紙箱		大紙箱	陸拾2

MC:

PC: Michael 4/21/04

品保: POC1 ACC

快遞簽收:

客戶簽收:

第一聯:物管存查 第二聯:會計存查 第三聯:客戶存查

PSWH-AC-001-14-B

裕沛科技股份有限公司

製表日期 2004/4/21

ADVANCED CHIP ENGINEERING TECHNOLOGY INC.

Die 出 貨 單

日期: 04/04/21 16:47:44

客戶名稱:	TwinMOS / 勤茂資通股份有限公司	出貨單號:	D04040011
送貨地點:	新竹縣湖口鄉自強路3號	運貨方式:	2.送達
送貨理由:	一般出貨		

項次	途程單號	託工單號	客戶批號	產品名稱	PART-NO	數量/單位	備註
011	E04030081	W45M0715	RET39500006	8-C2S56D30BP-A22G	Bin3	58 EA_Package	
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					總數:	5,556	

小紙箱		大紙箱	2

MC: Michael 4/21/04

PC:

品保: PQC 1 ACC

快遞簽收:

客戶簽收:

第一聯:物管存查 第二聯:會計存查 第三聯:客戶存查

PSWH-AC-001-14-B

中華民國專利證書

發明第 一七七七六六 號

發明名稱：晶圓型態擴散型封裝之製程

專利權人：裕沛科技股份有限公司

發明人：楊文媜、楊文彬

專利權期間：自中華民國 九十二 年 五 月 十一 日
至一一〇 年 九 月 二十四 日止

上開發明業經專利權人依專利法之規定取得專利權

經濟部智慧財產局
局長 蔡練生

中華民國 九十五 年 十一 月 五 日

注意：專利權人未依法繳納年費者，其專利權自屆期次日消滅。

CERTIFICATE OF PATENT, Taiwan, R. O. C.

Certificate No.: 177766

Title of Invention: Fan-Out Wafer Level Packaging

Proprietor(s): Advanced Chip Engineering Technology Inc.

Inventor(s): Wen-Kun Yang, Wen-Ping Yang

Patent Period: May. 11th, 2003 – Sep. 24th, 2021

This is to Certify that, in accordance with the Patent Law, a Patent has been granted to the proprietor(s) for the invention above.

Notice:
In case of the patentee's failure of effecting the payment of a patent annuity in accordance with the Patent Law, the invention patent right shall extinguish from the day following the expiration of the original statutory period for such payment.

Tsai Lien-sheng

Director-General

Intellectual Property Office, MOEA

September 5th, 2003

Amended Date:

Application Date: Sep. 25th, 2001	Serial No.: 90123655
Internal Class: H01L-23/02	

(Column above are filled by Taiwan IPO) Date:

Patent Application 531854

1. Title of Invention	Chinese	晶圓型態擴散型封裝之製程
	English	Fan-Out Wafer Level Packaging
2. Inventors	Name (Chinese)	1. 楊文焜 2. 楊文彬
	Name (English)	1. Wen-Kun Yang 2. Wen-Pin Yang
	Citizenship	1. Taiwan, R.O.C. 2. Taiwan, R.O.C.
	Home Address	1. No.47, Lane 6, Ankang St., Xian Shui Village, Hsinchu City 300, Taiwan (R.O.C.) 2. No.112, Jhulian St., Hsinchu City 300, Taiwan (R.O.C.)
3. Applicants	Name (Appellation) (Chinese)	1. 裕沛科技股份有限公司
	Name (Appellation) (English)	1. Advanced Chip Engineering Technology Inc.
	Citizenship	1. Taiwan, R.O.C.
	Business Address (Firm)	No. 65, Kuang-Fu North Rd., Hsin-Chu Industrial Park HU-KOU,, Hsin-Chu 303, Taiwan, R.O.C
	Name of Applicant's Representative (Chinese)	1. 楊文焜
	Name of Applicant's Representative (English)	1. Wen-Kun Yang

證據一

八、十	年 月 日 修正
申請日期：90.01.25	案號：90123655
類別：H01L-23/62	修正
（以上各欄由本局填註）	年 月 日 補充

發明專利說明書 531854

一、發明名稱	中文	晶圓型態損散型封裝之製程
	英文	
二、發明人	姓名（中文）	1. 楊文焜 2. 楊文彬
	姓名（英文）	1. 2.
	國籍	1. 中華民國 2. 中華民國
	住、居所	1. 新竹市仙水里18鄰安康街6巷47號 2. 新竹市竹蓮街112號
三、申請人	姓名（名稱）（中文）	1. 裕沛科技股份有限公司
	姓名（名稱）（英文）	1. Advanced Chip Engineering Technology Inc.
	國籍	1. 中華民國
	住、居所（事務所）	1. 新竹縣湖口鄉光復北路65號
	代表人姓名（中文）	1. 楊文焜
	代表人姓名（英文）	1.

四、中文發明摘要　(發明之名稱：晶圓型態擴散型封裝之製程)

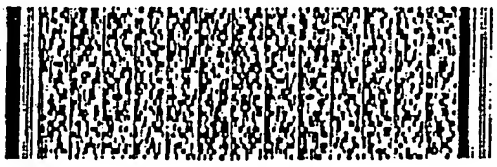
本發明是一種半導體封裝技術，特別是有關於利用擴散型(fan out)晶圓型態封裝製程製作封裝之方法。本發明包含切割晶粒後，經過篩選，將晶粒黏著於玻璃底座上，再將黏於晶粒上的金屬墊的I/O接頭透過特殊材質與方式，將I/O接頭植球的位置，以擴散型(fan out)方式，將接觸點往外擴散到晶粒的邊緣甚至晶粒的外圍，此種接觸點往外擴散，由於有較大的範圍來植入I/O植球，因此，一來可以增加I/O植球的數目，增加更多I/O接觸點，二來可以減少由於接觸點距(pitch)過於接近 所造 成的訊號干擾(signal coupling)及銲錫接頭過於接 近時造成的銲錫橋接(solder bridge)問題。本發明的特徵 是延用原來之封裝機台，不需額外花費，同時，本發明可 以應

英文發明摘要　(發明之名稱：)

四、中文發明摘要　(發明之名稱：晶圓型態掃散型封裝之製程)

用到8吋與12吋晶圓的封裝過程，又可以包含到晶粒與電容以及多晶粒(multi-chip)或多種 被動元件，例如中央處理器、DRAM, SRAM等等在封裝底座的封裝過程。此外，由於所選用的底做為玻璃底座，不會產生減少不同層之間，由於材質使用的不同所引發的應力不平衡問題，增加其可靠度。

英文發明摘要　(發明之名稱：)



本案已向

國(地區)申請專利	申請日期	案號	主張優先權
無			

有關微生物已寄存於

寄存日期	寄存號碼
無	

五、發明說明 (1)

發明領域：

本發明與一種半導體封裝有關，特別是有關於利用擴散型（fan out)晶圓型態封裝製程製作封裝之方法。

發明背景：

隨著電子元件尺寸的縮小化後，在積體電路的製造過程上出現許多新挑戰。且由於電腦以及通訊技術之迅勃發展，伴隨需要的是更多不同種類與應用之電子元件。例如，由語音操作之電腦界面或其他通訊之界面均需要許多之記憶元件以及不同類型之半導體元件。是故，積體電路之趨勢仍然會朝向高積集度發展。隨著半導體技術之快速演進，電子產品在輕薄短小、多功能速度快之趨勢的推動下，IC半導體的I/O數目不但越來越多密度亦越來越高，使得封裝元件的引腳數亦隨之越來越多，速度的要求亦越來越快。半導體晶片通常個別地封於塑膠或陶瓷材料之封裝體之內。封裝體之結構必須可以保護晶片以及將晶片操作過程中所產生之熱散出，傳統之封裝亦被用來作為晶片功能測試時之用。

早期之封裝技術主要以導線架為主之封裝技術，利用引腳做為訊號之輸入以及輸出。而在高密度輸入以及輸出端之需求之下，導線架之封裝目前已不符合上述之需求。目前，在上述之需求之下，封裝也越做越小以符合目前之趨勢，而高密度輸出/輸入端（I/O)之封裝也伴隨球矩陣排

五、發明說明 (2)

列封裝技術（ball grid array;以下簡稱BGA封裝）之發展而有所突破，因此，IC半導體承載的封裝趨向於利用球矩陣排列封裝技術（BGA）。BGA構裝的特點是，負責I/O的引腳為球狀較導線架封裝元件之細長引腳距離短且不易受損變形，其封裝元件之電性的傳輸距離短速度快，可符合目前及未來數位系統速度的需求。例如，於美國專利U. S. Patent No.5629835，由Mahulikar等便提出一種BGA之結構，發明名稱為"METAL BALL GRID ARRAY PACKAGE WITH IMPROVED THERMAL CONDUCTIVITY"。又如美國專利U. S. Patent No. 5,239,198揭露一種封裝形式，此封裝包含一組裝於印刷電路板上之基板，基板利用FR4材質組成，該基板上具有一導電線路形成於基板之一表面。

此外，目前已經有許多不同型態之半導體封裝，不論是哪一種型態之封裝，絕大部分之封裝為先行切割成為個體之後再進行封裝以及測試。而美國專利有揭露一種晶圓型態封裝，請參閱，US5323051，發明名稱為"Semiconductor wafer level package"。此專利在切割晶粒之前先行進行封裝，利用玻璃當作一黏合材質使得元件封於一孔中。一遮蓋之穿孔做為電性連結之通道。因此，晶圓型態封裝為半導體封裝之一種趨勢。另外所知之技術將複數晶粒形成於半導體晶圓之表面，玻璃利用黏著物質貼附於晶圓之表面上。然後，沒有晶粒的那一面將被研磨以降低其厚度，通常稱做背面研磨（back

五、發明說明 (3)

grinding)。接著，晶圓被蝕刻用以分離IC以及暴露部分之黏著物質。

此外，以往之封裝技術領域中，I/O鋁墊部分是接於晶粒的表面，由於晶粒面積有限，I/O鋁墊在該有限面積下，將限制其鋁墊數目。再者，I/O鋁墊之間距過小將會造成訊號間的耦合(signal coupling)或訊號間的干擾。

由於晶圓型態封裝將成為封裝技術之趨勢，本發明的主要特徵是取代以往晶粒表面上I/O植球的位置，以擴散型(fan out)方式，將接觸點往外擴散以提升較大的範圍來植入做為I/O之植球，因此，其優點包含可以增加I/O植球的數目，亦即增加更多I/O，或是在晶粒朝向縮小化之趨勢下，保持I/O之最小間距(pitch)以防止過於接近所造成的訊號干擾(signal coupling)與銲錫接頭過於接近所造成的銲錫橋接(solder bridge)問題。

發明目的及概述：

本發明之目的為提供一晶圓型態擴散型封裝之方法。

本發明之另一目的為提供一種晶圓型態封裝以及其製程。

本發明之晶圓型態封裝製程包含提供，將切割過之晶圓經過篩選通過品質管制後的晶圓，選取好的晶粒

五、發明說明 (4)

(die)，透過吸取與放置的動作重新排列於一新的玻璃底座。並經由黏著劑(adhesion)將各個晶粒黏著於上述底座上。晶粒擺置於玻璃底座上，使晶粒間的距離(pitch)加大，其目的是希望在後續封裝過程中多出來的空間能夠容納擴散型(fan out)圓錫球陣列(ball array)。此擴散型封裝技術可以提昇I/O數目，或是在晶粒尺寸縮小情形下，仍保持其理想間距(pitch)以防止I/O間之訊號干擾。將進行封裝之晶圓正面(或第一表面)具有做為輸入輸出之金屬墊，例如鋁墊(I/O pad or aluminum pad)，該金屬墊是做為內連線(inter connect)之用，而且是利用光罩(mask)經過校準(alignment)、曝光與顯影(developer)過程形成於晶圓的上面。先行在晶圓與鋁墊的上面透過旋轉塗佈機(spin coater)旋塗(spin coating)一層BCB絕緣層。接著，去除部分的BCB，形成第一開口(opening)以曝露出下方的金屬鋁墊。接著，於鋁墊表面形成一化鎳/化金(Ni/Au)膜層。接著，再將晶圓切割以形成個別之晶粒單體。接著，將上述之晶粒經由篩選與品質檢驗合格後經由具有吸附與放置功能的機械將晶粒配置於玻璃底座上面以黏著物固定，並予以固化。

接著，全面性地填充一層第一環氧樹脂(EPOXY)於玻璃底座、晶粒、BCB與開口的鋁墊的上面。然後，經過光阻型蝕刻或化學藥劑以移除鋁墊上方的第一環氧樹脂，形成第二開口暴露鋁墊。接著，在爐(oven)內予以固化此第一環氧樹脂。接著，用銲錫(solder)以網印(printer)技

五、發明說明 (5)

術填滿該第二開口。

然後，再上一層鈦/銅(Ti/Cu)於銲錫(soldcr)的上面。接著，在鈦/銅層上面以朝外擴散(fan out)的方式，電鍍(plating)一定面積的銅導線，銅導線的位置，一端是與鋁墊切齊，另一端以水平向方向朝外擴散(fan out)的方式牽引導線。在定義銅導線之光阻去除前，先電鍍一化鎳或化金，之後去除光阻。然後蝕刻鈦/銅。接著，全面性地塗佈(coating)一層第二環氧樹脂(epoxy)於銅導線與下層環氧樹脂的上面，並以固化之步驟利用紫外線照射或加熱處理以硬化上述之第二環氧樹脂。

然後，去除銅導線上面的部分第二環氧樹脂(epoxy)並形成第三開口，其位置儘可能位於銅導線的外側(遠離鋁墊的一邊)以利於製作擴散型(fan out)I/O結構。

接下來的步驟是，在第三開口上面形成一層鎳(Ni)層，接著在第三開口處，鎳(Ni)層的上面，透過網印技術或植球技術，植入焊錫球(solder ball)，焊錫球經過此一封裝過程設計後的位置，並不在金屬墊的正上方，而是水平向側沿伸到金屬墊的側邊上。最後，完成切割晶粒與底座玻璃的步驟。

本發明之結構如下：

一種晶圓型態擴散型封裝包含：絕緣基座；晶粒配置於該絕緣基座之上，其中晶圓包含複數個鋁墊形成於其上；BCB層，塗佈於晶粒表面，並具有複數第一開口暴露

五、發明說明 (6)

複數鋁墊；銲錫填充於第一開口；第一環氧樹脂，塗佈於晶粒、絕緣基座以及BCB層之上；銅導線配置於第一環氧樹脂並與銲錫連接；第二環氧樹脂塗佈於銅導線之上並具有第二開口暴露部分之銅導線；錫球配置於第二環氧樹脂之上並填入該第二開口與該銅導線連接。

其中更包含銅種子層形成於第一銲錫之上，銅種子層包含鈦/銅(Ti/Cu)或鎳/銅(Ni/Cu)。其中更包含阻障或黏著層形成於鋁墊之上，阻障或黏著層之材質組成包含鎳/金(Ni/Au)。而錫球與該銅導線之介面包含鎳(Ni)。本發明將上述結構之封裝稱為ACE BGA。

發明詳細說明：

本發明揭露一種晶圓型態封裝(wafer level packaging, WLP)以及製作晶圓型態封裝之方法，詳細說明如下，所述之較佳實施例只做一說明非用以限定本發明，首先參閱圖一，將經過測試以及切割過之晶圓經過篩選通過品質管制後 的晶粒，選 取測試 合格之晶粒(die) 1a，透過吸取與放置裝置將其重新排列配置於一新的玻璃底座1(該底座可以是玻璃、陶瓷或矽晶)，並經由黏著劑(adhesion)將各個晶粒黏著於上述底座1上，該黏著劑厚度大約10μm，該固化黏著劑的過程是利用旋塗機(spin coater)進行黏著動作。晶粒擺至於玻璃底座上，晶粒間

五、發明說明 (7)

的距離(pitch)加大，其目的是希望在後續封裝過程中具有充足之空間能夠容納擴散型(fan out)圓錫球陣列(ball array)。此擴散型封裝技術可以提昇I/O數目，或是在晶粒尺寸縮小情形下，仍保持其理想間距(pitch)以防止I/O間之訊號干擾。封裝的大小面積取決於後續製程完成後擴散型(fan out)圓錫球陣列(ball array)之間的間距(pitch)大小而定。在另一實施例中，該玻璃基座1上也可以包含電容(capacitor)1b配置於晶粒之側，以提升濾波效果，如圖二所示。

以下所述封裝過程是從具有金屬墊(metal pad)的單一晶粒開始其封裝過程：

圖三中，將進行封裝之晶圓2正面(或第一表面)具有做為輸入輸出之金屬墊，例如鋁墊(I/O pad or aluminum pad)4，該金屬墊是做為內連線(inter connect)之用，利用光罩(mask)經過校準(alignment)、曝光與顯影(developer)過程，將金屬墊形成於晶粒的上面。接著，在晶圓上透過旋轉塗佈機(spin coater)旋塗(spin coating)一層BCB絕緣層8於晶粒2與鋁墊4的上面以保護晶粒，BCB的厚度大約為5-10μ m。

接著，經過光罩(mask)校準(alignment)、曝光與顯影(developer)過程以去除部分的BCB 8，形成第一開口(opening)9以曝露出下方的金屬鋁墊4，值得注意的是，此切割道(scribe line)上亦被暴露且大於其切割道之寬

五、發明說明 (8)

度，以利於切割時不損及BCB，如圖四所示。之後以電鍍方式形成化鎳或化金 11於鋁墊 4之上。

經過切割，如圖五表示，將複數個晶粒 2a(此處晶圓業經切割形成晶粒)經白篩選與品質檢驗合格後經由具有吸附與放置功能的機械將晶粒 2a擺置於玻璃底座 6上面，並透過黏著劑 7黏著於玻璃底座 6上面，接著在爐 (oven)內予以固化 (curing)。

接著，全面性地在玻璃底座 6、晶粒 2a、BCB 8與開口的鋁墊 4的上面全面性地填充一層第一環氧樹脂 (EPOXY) 10。接著，如圖六至圖七所示，經過光阻型蝕刻或化學藥劑以移除鋁墊 4上方的第一環氧樹脂 10，形成第二開口 13，並曝露出下方的鋁墊 4。接著，在爐 (oven)內予以固化，此第一環氧樹脂 10，其厚度大約為 10-25μ m之間 (這裡的厚度指的是在晶粒表面上的厚度)。

接著，接著將剩餘的環氧樹脂，以RIE電漿清潔晶粒 2a表面。至於上述的剩餘的環氧樹脂則以 10 表示。上述之鎳 /金 (Ni/Au)或化鎳層 11可做為阻障層或是黏著層之功用。

接著，在鎳 /金 (Ni/Au)或化鎳層 11上方的第二開口 13內利用銲錫 (solder)12以網印 (printer)技術填滿該第二開口 13。接著，以紅外線 (IR)迴流 (reflow)固化 (curing)此銲錫 (solder)12，然後，全面性地濺鍍一層鈦 /銅 (Ti/Cu)19於剩餘的環氧樹脂 10 與銲錫 (solder)12的上面，以作為銅種子層 (seeding layer)，如圖八所示。

五、發明說明 (9)

接著，如圖九所示，以光阻（未圖示）定義銅導線圖案，利用電鍍方式形成銅導線於鈦/銅（Ti/Cu）19的上面，一端對準第二開口銲錫12的內端（晶粒的內側邊），而另一端以水平向方向朝外擴散（fan out）的方式（晶粒的內側邊），明確的講，也就是說銅導線14的位置，一端是與鋁墊4切齊，另一端以水平向方向朝外擴散（fan out）來牽引導線，其與下層環氧樹脂10及銲錫12的接觸面積較鋁墊4的開口來的大，其目的主要是用來增加I/O的植球區域面積，接著，在銅導線14上面形成一層化鎳（Ni）層或化金層17以做為後續銲錫植球的黏著層，再移除光阻。並移除曝露於剩餘環氧樹脂10的上面部分鈦/銅（Ti/Cu）19。

接著，如圖十所示，全面性地塗佈（coating）一層第二環氧樹脂（epoxy）16於銅導線14、鎳（Ni）層17與下層環氧樹脂10的上面，並以固化之步驟利用紫外線照射或加熱處理以硬化上述之第二環氧樹脂（epoxy），防止銅導線14被氧化。

接著，如圖十一所示，去除銅導線14與鎳（Ni）層17上面的部分第二環氧樹脂（epoxy）16並形成第三開口15，該第三開口15的位置是在銅導線14與鎳（Ni）層17的上面，且儘可能位於銅導線14的外側（遠離鋁墊4的一邊）以利於製作擴散型（fan out）I/O結構。

接著，如圖十二所示，接著在第三開口15處，鎳（Ni）層17的上面，透過網印技術或植球技術植入焊錫球（solder ball）18，由圖中明顯可見，焊錫球18經過此一

五、發明說明 (10)

封裝過程設計後的位置，並不在金屬墊4的正上方，而是水平向側伸到金屬墊4的側邊上。

接著，如圖十三所示，再經過紅外線(IR)迴流(reflow)烘烤(curing)環氧樹脂，晶圓再傳送至晶圓型態測試裝置中進行晶圓型態測試，例如最後測試(final testing)以及切割(sawer)過程，並切割晶粒與晶粒間切割線(scribe line)20與玻璃基座6，以分離個別之封裝體。

本發明之製程較先前技術簡單，在未分割前以晶圓型態進行測試，且在測試後可以沿著切割道切割成個別之晶粒，以吸取放置裝置被置於玻璃基板之上完成晶圓型態擴散型封裝(wafer level fan out packaging)。

圖十四所示，為鎳/金(Ni/Au)或化鎳層11、鈦/銅(Ti/Cu)或鎳/銅(Ni/Cu)19、鎳(Ni)層17各黏著層(glue layer)與阻障層，在內連線的各個位置示意圖。

圖十五所示，為單一晶粒的晶圓型態擴散型封裝(wafer level fan out packaging)成型的剖面圖。本發明也能將晶粒電容2b納入封裝過程，圖十六所示，即為電容2b植入到玻璃基座上與單一晶粒的晶圓型態擴散型封裝(wafer level fan out packaging)的成型剖面圖。在另一實施例中，本發明也能將多晶粒(multi-chip)或多種被動元件整合納入封裝過程，圖十七所示，即為多晶粒(multi-chip)的封裝過程中晶圓型態擴散型封裝(wafer level fan out packaging)的剖面圖，圖中2a、2c即代表不同之晶粒，此種封裝方式可將多晶粒與多種被動元件整合封裝，形成系

五、發明說明 (11)

統式封裝 (system in package)。

本發明的主要特徵是植基於晶圓型態封裝，並使用擴散型 (fan out)方式將晶粒表面上 I/O植球的位置側向延伸，其優點可以增加 I/O植球的數目；可以減少由於接觸點距 (pitch)過於接近所造成的訊號干擾問題。

本發明的主要優點如下：

1.如圖一所示，本發明之晶圓型態封裝之成本較傳統技術低，再藉由已測試及切割過之晶圓經過篩選，將通過品質管制後的晶粒，選取好的晶粒 (die)，透過吸取與放置的動作重新排列於一新的玻璃底座，可以減少製作成本完成擴散型封裝。

2.由於尺寸縮小原則，晶粒 (chip)亦隨之縮小，而為了使得晶粒間的距離 (pitch)仍然保持理想的距離 (以不影響到訊號傳遞耦合為原則)，在本發明中是以晶圓型態擴散型封裝 (wafer level fan out packaging)，將 I/O線向外擴散，並將連線拉到晶粒外的區域，以增加銲錫圓球的數目及維持理想晶粒間的距離 (pitch)。

3.本發明可以應用到 8吋與 12吋晶圓的封裝過程。

4.本發明可以整合晶粒與電容於同一封裝單體。

5.本發明能將多晶粒 (multi-chip)或多種被動元件整合於同一單體，例如中央處理器、DRAM, SRAM等等在封裝底座的封裝過程。

6.本發明能將環氧樹脂中之銲錫當作緩衝區 (buffer zone)，在後續製程中，減少不同層之間，由於材質使用

五、發明說明 (12)

的不同所引發的應力不平衡問題，增加其可靠度(reliability)。

7.本發明的底座是玻璃，其材質與晶粒底材相同，由於材質中均含有矽材質，兩者具有同樣的熱力膨脹係數(thermal coefficient of expansion, TCE)，不會產生應力不平衡現象。

8.本發明的底座可以使用玻璃、灰石與矽晶(glass, ceramic, silicon)以改善其可靠度。

9.本發明的封裝機械部是以現有機械設備進行封裝，可以省去額外添購的費用。

10.本發明可以增加銲錫圓球的數目，其中有些銲錫圓球當作樣本假輸出輸入端(dummy ball)，此dummy ball雖無訊號傳遞之功能卻可供作緩衝區(buffer zone)以減弱不同材質間的應力，減少封裝時晶粒龜裂的現象發生。

本發明以較佳實施例說明如上，而熟悉此領域技藝者，在不脫離本發明之精神範圍內，當可作些許更動潤飾，其專利保護範圍更當視後附之申請專利範圍及其等同領域而定。

圖式簡單說明

圖式簡單說明：

本發明的較佳實施例將於往後之說明文字中輔以下列圖形做更詳細的闡述：

圖一為晶圓級封裝單一晶粒自晶圓切割後厚擺置於玻璃底座之示意圖。

圖二為晶圓級封裝具有電容的晶粒自晶圓切割後擺置於玻璃底座之示意圖。

圖三所顯示為本發明中具有金屬墊的晶粒的表面上形成一層BCB保護層之示意圖。

圖四所顯示為本發明中去除部分BCB保護層之示意圖。

圖五所顯示為本發明中，晶粒經過吸附與放置後黏至於底座之示意圖。

圖六所顯示為本發明中，全面性地填充一層第一環氧樹脂之示意圖。

圖七所顯示為本發明中，經過光阻型蝕刻或化學藥劑以移除鋁墊上方的第一環氧樹脂之示意圖。

圖八所顯示為本發明中，用銲錫(solder)以網印(printer)技術填滿該第二開口之示意圖。

圖九所顯示為本發明中，顯示為透過校準、曝光與顯影電鍍(plating)一定面積的銅導線之示意圖。。

圖十所顯示為本發明中，為全面性地塗佈(coating)一層第二環氧樹脂(epoxy)之示意圖。

圖十一所顯示為本發明中，去除銅導線上面的部分第二環

圖式簡單說明

氧樹脂（epoxy）16並形成第三開口之示意圖。

圖十二所顯示為透過網印技術或植球技術，植入焊錫球之示意圖。

圖十三所顯示為切割晶粒與晶粒間切割線與玻璃基座之示意圖。

圖十四所顯示為晶粒上各阻障層的相關位置示意圖。

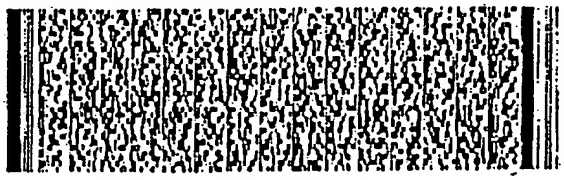
圖十五所顯示為單一晶粒的晶圓型態擴散型封裝成型的剖面圖。

圖十六所顯示為電容植入到玻璃基座上與單一晶粒的晶圓型態擴散型封裝的成型剖面圖。

圖十七所顯示為為多晶粒的封裝過程中晶圓型態擴散型封裝的剖面圖

元件符號對照

晶粒	1a
電容	1b
晶圓	2
晶粒	2a
電容	2b
晶粒	2c
鋁墊	4
玻璃底座	6
黏著劑	7
BCB絕緣層	8



圖式簡單說明

環氧樹脂　10

剩餘的環氧樹脂 10'

化鎳 /化金　11

銲錫　12

第二開口　13

銅導線　14

環氧樹脂　16

鎳層　17

焊錫球　18

鈦 /銅　19

晶粒間切割線　20

六、申請專利範圍

申請專利範圍：

1.一種晶圓型態擴散型封裝之製程，該晶圓型態擴散型封裝之製程包含：

提供具有複數晶粒形成於其上之晶圓；

測試該晶圓上之複數晶粒並標記合格之晶粒；

旋塗BCB絕緣層以保護該晶粒；

去除部分的該BCB層，形成第一開口以曝露出該晶粒上之金屬鋁墊；

切割該晶圓以分離該複數晶粒；

經篩選通過品質管制後的晶粒，透過吸取與放置的動作重新排列配置黏著於一絕緣底座之上；

全面性地填充一層第一環氧樹脂於該絕緣底座、該晶粒、該BCB與該第一開口的該鋁墊上；

蝕刻以移除該鋁墊上方的該第一環氧樹脂，形成第二開口；

固化該第一環氧樹脂；

濺鍍一阻障層於該該鋁墊的上；

以網印(printer)技術用銲錫在該阻障層上並填滿該第二開口；

形成銅種子層於銲錫及第一環氧樹脂之上；

利用一光阻電鍍一定面積的銅導線於該銲錫與該阻障層之上；

形成化鎳或化金於銅導線之上；

六、申請專利範圍

去除光阻；

全面性地塗佈（coating）一層第二環氧樹脂（epoxy）於該銅導線之上；

固化上述之該第二環氧樹脂；

去除該銅導線上部分該第二環氧樹脂並形成第三開口；

植入焊錫球於該第三開口；以及

切割該絕緣基座用以分離個別封裝單體。

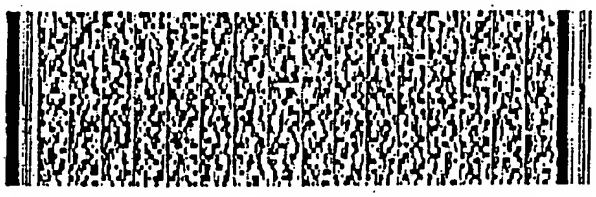
2.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，其中在形成上述銅導線之前更包含濺鍍一銅種子層於該銲錫與該第一環氧樹脂上面。

3.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，其中該黏著晶粒於該底座的過程，更包含在爐內予以固化該黏著劑。

4.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，其中該BCB絕緣層之厚度大約為5-25μm。

5.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，其中該蝕刻該第一環氧樹脂，以形成該第二開口的過程，是藉由光阻型蝕刻或化學藥劑進行。

6.如申請專利範圍第5項之晶圓型態擴散型封裝之製程，



六、申請專利範圍

其中形成上述第二開口之後，更包含以RIE電漿清洗晶粒表面。

7.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，該阻障層之材料包含鎳/銅或化鎳層。

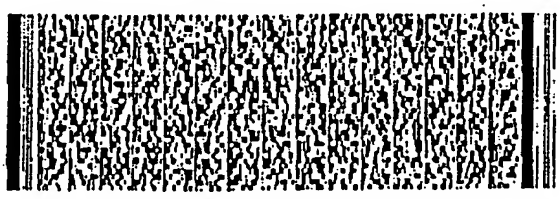
8.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，完成上述網印(printer)技術後，更包含以紅外線(IR)迴流固化該銲錫。

9.如申請專利範圍第2項之晶圓型態擴散型封裝之製程，其中上述之銅種子層包含鈦/銅。

10.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，其中固化該第二環氧樹脂之步驟係包含利用紫外線照射或加熱處理。

11.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，其中上述植入於該第三開口的之焊錫球係採用網印技術或植球技術。

12.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，其中更包含電容配置於該晶粒之側並排於該玻璃底座上。



六、申請專利範圍

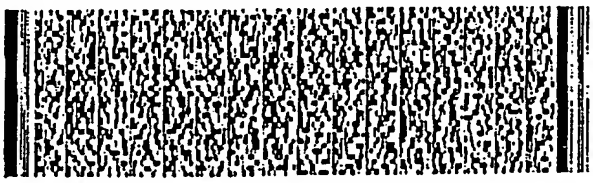
13.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，其中更包含另一晶粒配置於該晶粒之側並排於該玻璃底座上，形成多晶粒(multi-chip)封裝結構，該另一晶粒包含但不限於CPU, DRAM, SRAM等元件。

14.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，其中上述絕緣底座包含玻璃。

15.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，其中上述絕緣底座包含陶瓷。

16.如申請專利範圍第1項之晶圓型態擴散型封裝之製程，其中上述絕緣底座包含矽晶。

17.一種晶圓型態擴散型封裝，包含：
絕緣基座；
晶粒，配置於該絕緣基座之上，其中該晶圓包含複數個鋁墊形成於其上；
BCB層，塗佈於該晶粒表面，並具有複數第一開口暴露該複數鋁墊；
銲錫，填充於該第一開口；
第一環氧樹脂，塗佈於該晶粒、該絕緣基座以及該BCB層之上；
銅導線，配置於該第一環氧樹脂並與該銲錫連接；



六、申請專利範圍

第二環氧樹脂，塗佈於該銅導線之上，並具有第二開口暴露部分之該銅導線；及

錫球，配置於該第二環氧樹脂之上並填入該第二開口與該銅導線連接。

18.如申請專利範圍第17項之晶圓型態擴散型封裝，其中更包含銅種子層形成於該第一銲錫之上。

19.如申請專利範圍第18項之晶圓型態擴散型封裝，其中上述銅種子層包含鈦/銅（Ti/Cu）。

20.如申請專利範圍第18項之晶圓型態擴散型封裝，其中上述銅種子層包含鎳/銅（Ni/Cu）。

21.如申請專利範圍第17項之晶圓型態擴散型封裝，其中更包含阻障或黏著層形成於該鋁墊之上。

22.如申請專利範圍第21項之晶圓型態擴散型封裝，其中該阻障或黏著層包含鎳/鋁（Ni/Al）。

23.如申請專利範圍第17項之晶圓型態擴散型封裝，其中該錫球與該銅導線之介面包含鎳（Ni）。

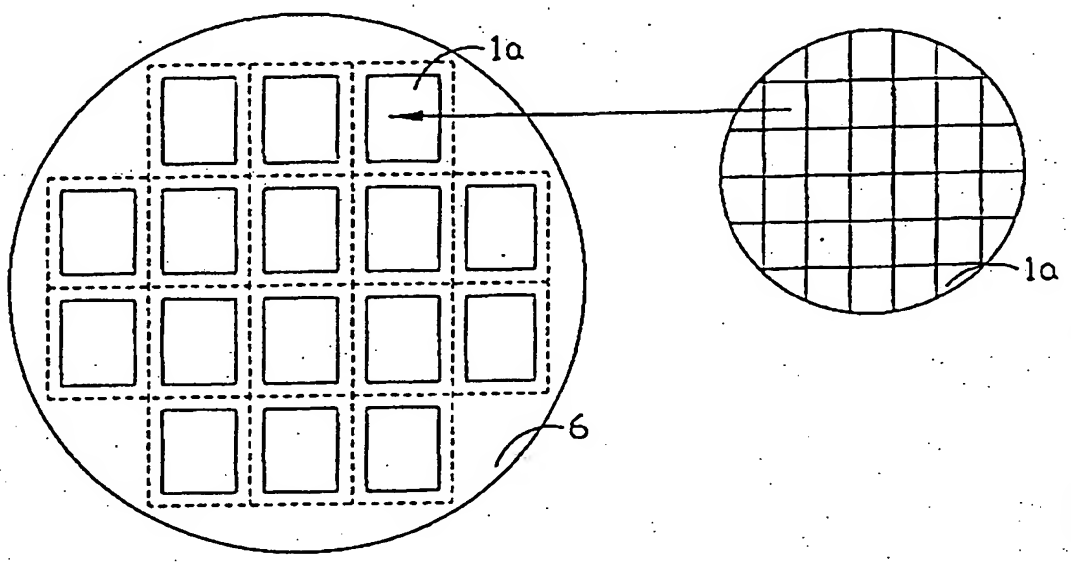
24.如申請專利範圍第17項之晶圓型態擴散型封裝，其中

六、申請專利範圍

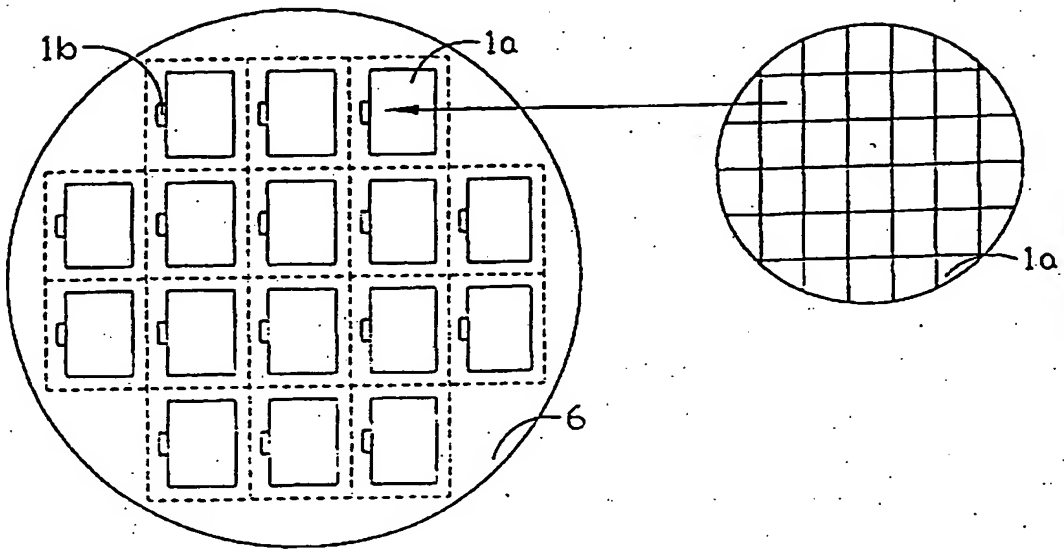
更包含一電容配置於該晶粒之側。

25.如申請專利範圍第17項之晶圓型態擴散型封裝，其中更包含另一晶粒配置於該晶粒之側。

圖式

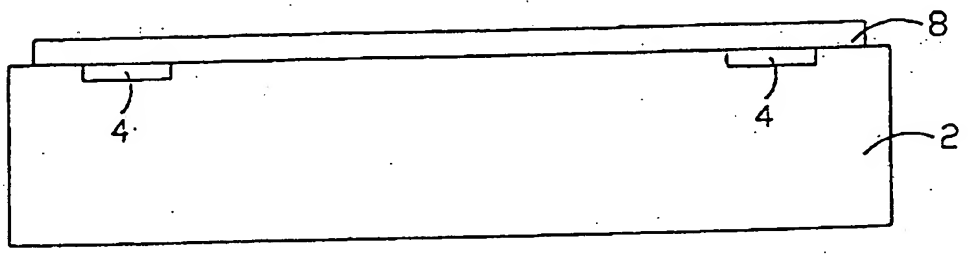


圖一



圖二

圖式



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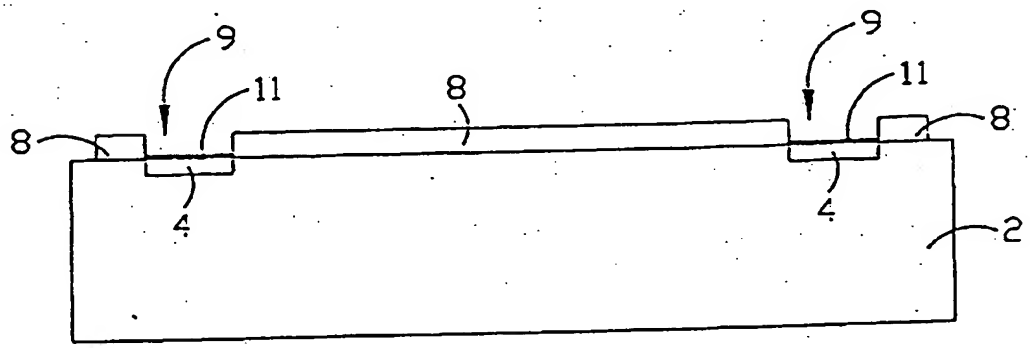
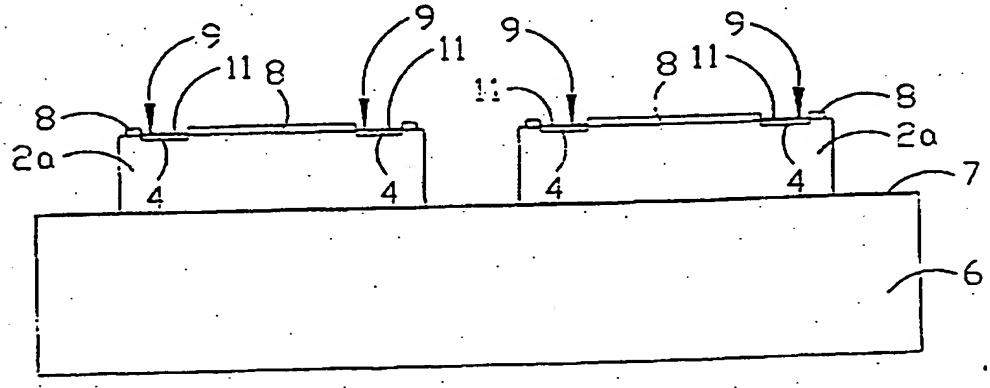
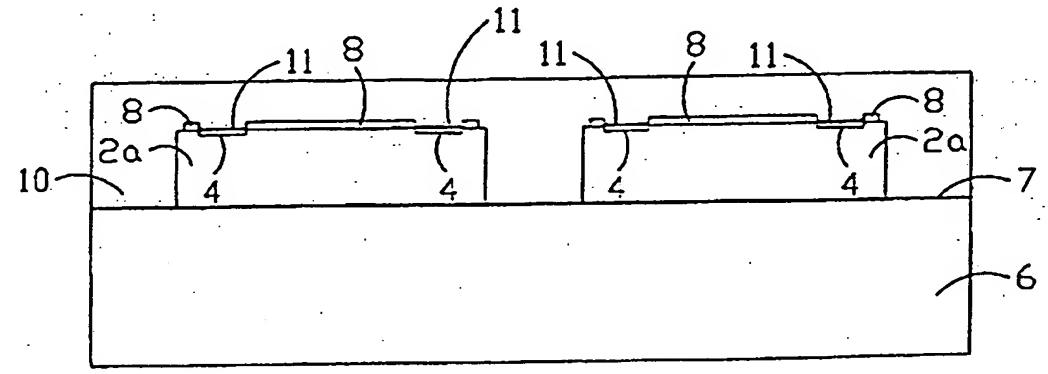


圖四



圖五

圖式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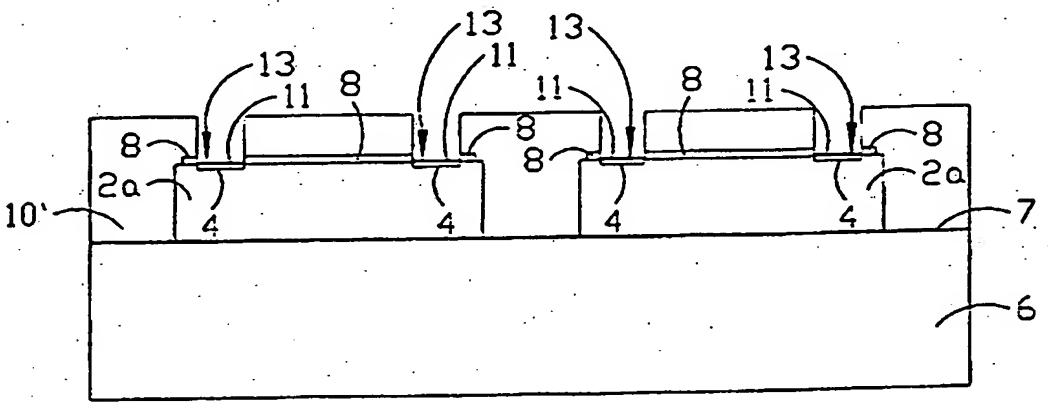
圖六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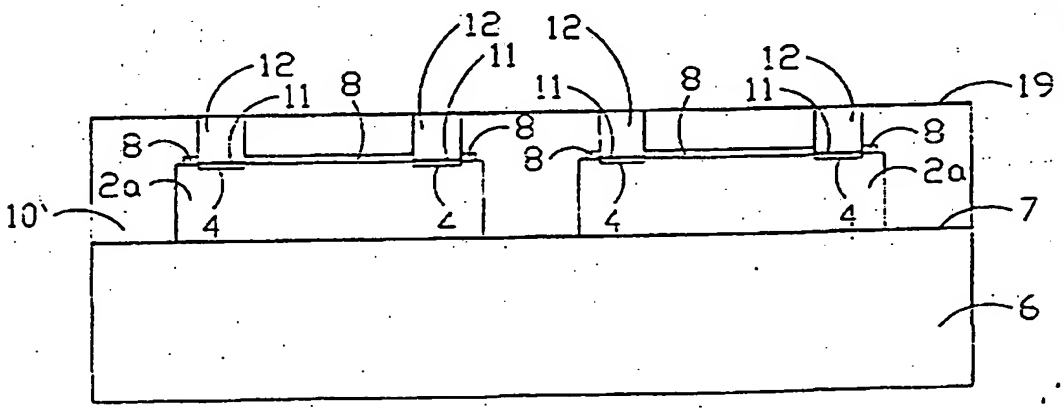
圖七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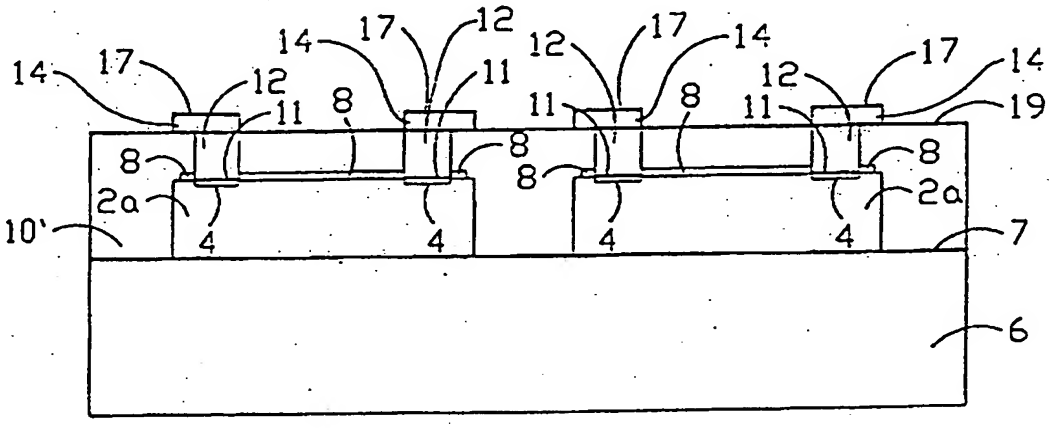
圖八

圖式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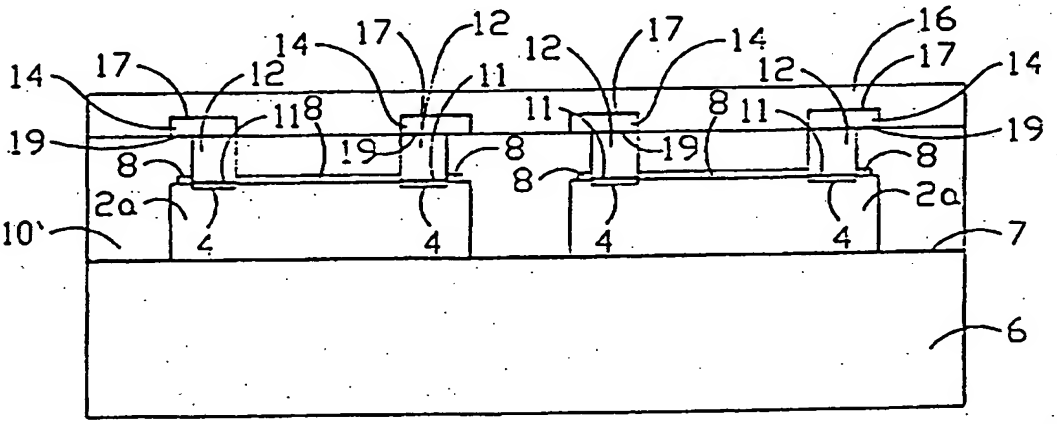
圖九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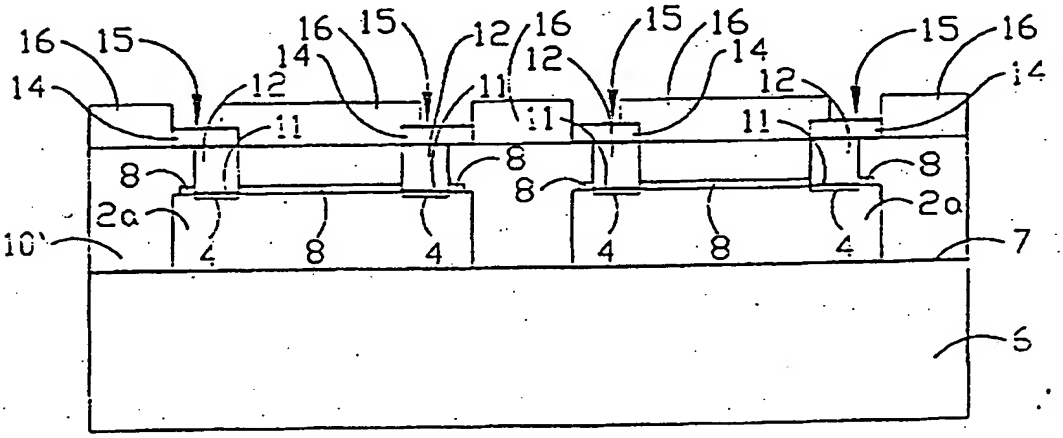
圖十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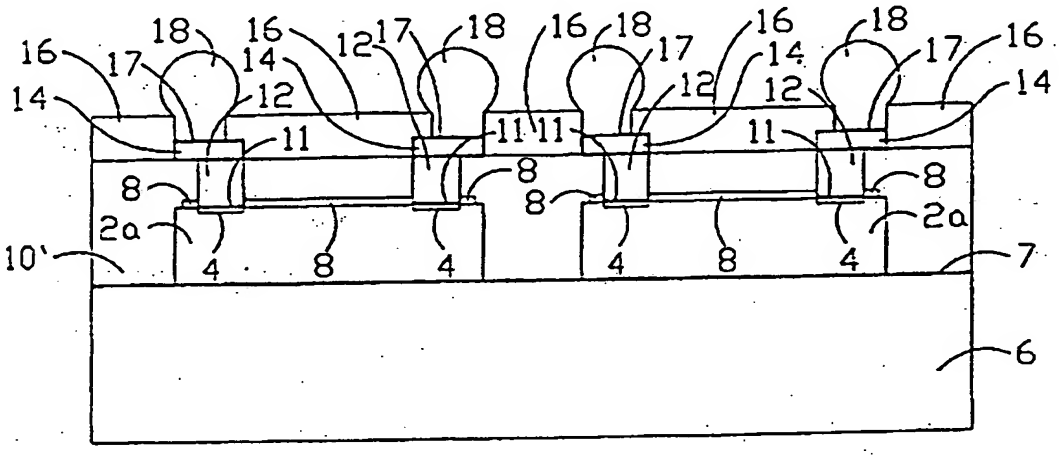
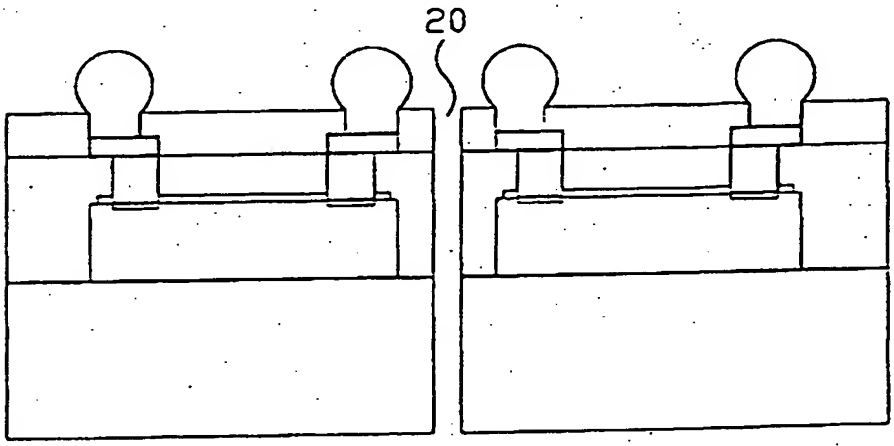
圖十一

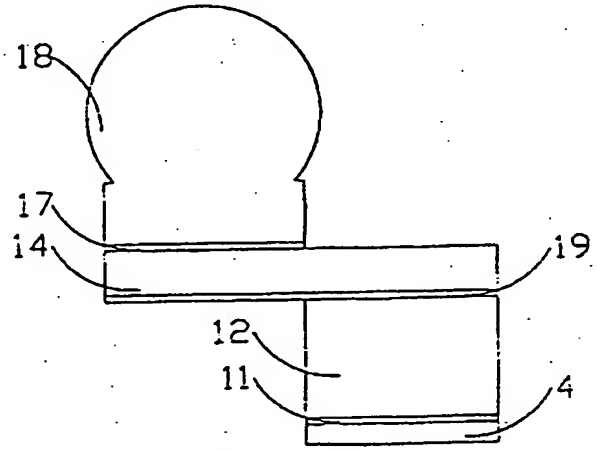
圖式



圖十二

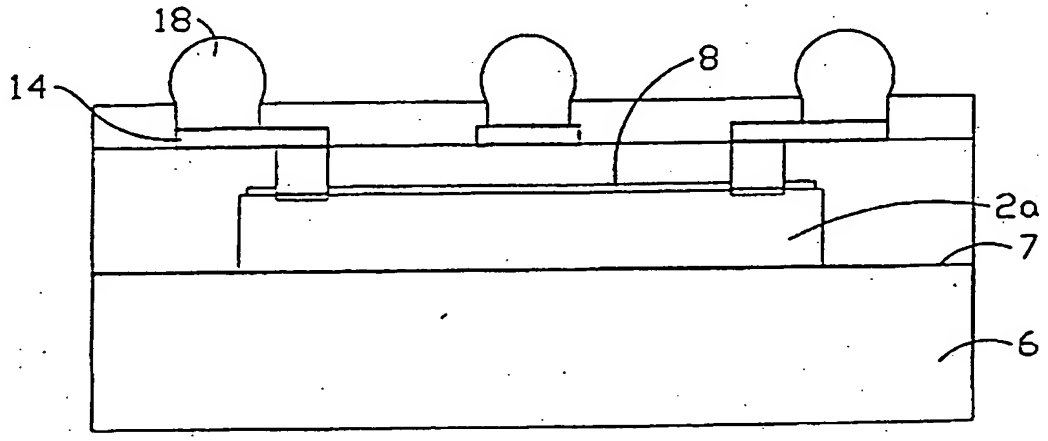


圖十三



圖十四

圖式



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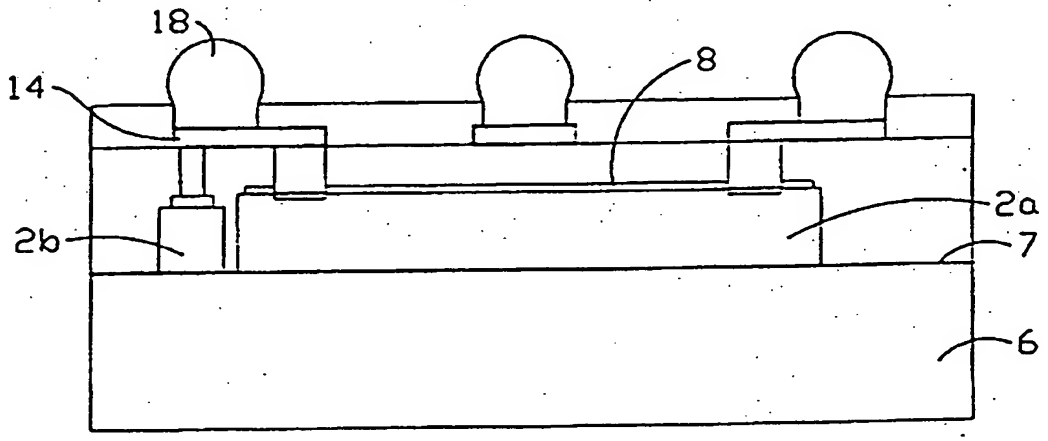
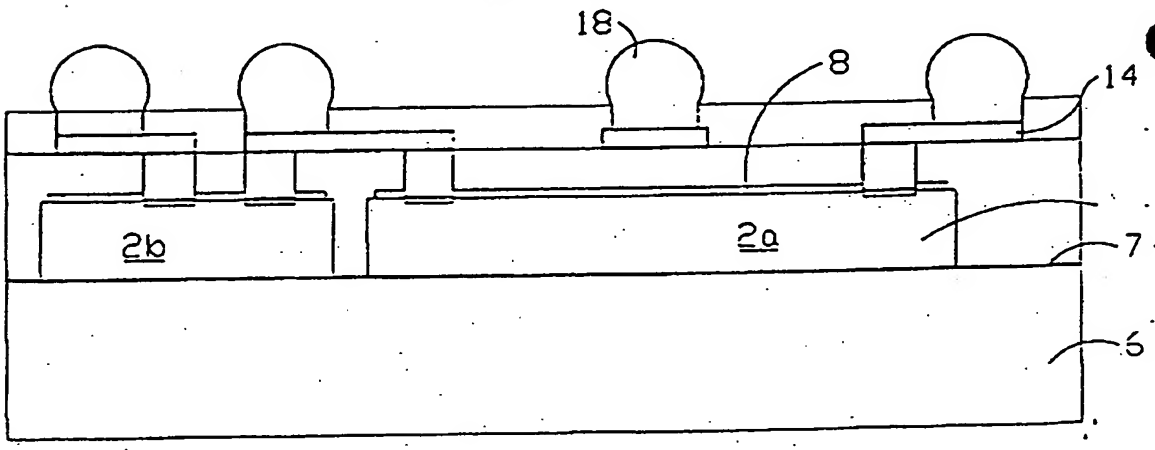


圖十六



圖十七